

Video Time Stamp	Cadence PCB Configuration Matrix	Orcad PCB Designer Standard	Orcad PCB Designer Professional	Allegro PCB Designer
	SCHEMATIC ENTRY + DATA MANAGEMENT			
	Allegro Design Authoring (DE HDL) (ADA)			✓
	Graphical, flat, and hierarchical page editor	✓	✓	✓
3.2	OrCAD Capture Market place	✓	✓	✓
1.02	Net Groups	✓	✓	✓
2.25	Intelligent PDF - Capture or Capture CIS	✓	✓	✓
0.49	AutoWire	✓	✓	✓
0.33	3D Footprint Viewer	✓	✓	✓
2.2	Coloured Components / nets	✓	✓	✓
	Capture Market Place for apps and scripts	✓	✓	✓
	Tcl TK scripting support	✓	✓	✓
	Online design rule check	✓	✓	✓
	Forward- and back-annotation of properties / pin-and-gate swaps	✓	✓	✓
	Graphical schematic part and library editor	✓	✓	✓
0.08	Cross-probing and cross-placing PCB Editor	✓	✓	✓
	FPGA design-in / pin import & export	✓	✓	✓
	Multiple PCB netlist interfaces	✓	✓	✓
	Property editor for pins, components, nets	✓	✓	✓
1.13	Component Information Management system	CIS option	CIS option	✓
	ODBC-compliant component database	CIS option	CIS option	✓
	Interface to relational database and management systems	CIS option	CIS option	✓
	Centralized part number and information management system	CIS option	CIS option	✓
1.13	Database query for part selection and parametric properties	CIS option	CIS option	✓
2.48	Assembly variations on a fabricated PCB	CIS option	CIS option	✓
2.48	BOM Variants Manager	CIS option	CIS option	✓
1.35	ActiveParts.com over 2,000,000 schematic parts ready to place CIS only	CIS option	CIS option	✓
	Part substitutions and part "not present" definable per variation	CIS option	CIS option	✓
1.54	Part search DIGIKEY, FARNELL, FUTURE, NEWARK, MOUSER, ARROW not ADA	CIS Option + CIP E Option	CIS Option + CIP E Option	CIP E Option
7.12	SIGNAL INTEGRITY	Orcad PCB Designer Standard	Orcad PCB Designer Professional	Allegro PCB Designer
	Pre- & Post-route signal integrity analysis		✓	
	Graphical topology definition and exploration		✓	
	Interactive waveform viewer		✓	
	Macro modelling support (DML)		✓	
	BIS 5.0 support		✓	
	IBIS ICM model support		✓	
	Spectre-to-DML		✓	
	HSPICE-to-IBIS		✓	
	Lossy transmission lines		✓	
	Coupled (3 net) simulation		✓	
	Differential pair exploration and simulation		✓	
7.02	ROUTER	Orcad PCB Designer Standard	Orcad PCB Designer Professional	Allegro PCB Designer
	6 Signal Layer limit		✓	✓
	Shape-based or Gridded routing		✓	✓
	SMD Fanout		✓	✓
	Trace Width by Net and Net Classes		✓	✓
	45-degree / Memory Pattern Routing		✓	✓
	Interactive Routing with Shoving and Plowing		✓	✓
	Interactive Floorplanning		✓	✓
	Online Design Rule Checking		✓	✓
	Flip, Rotate, Align, Push, and Move Components		✓	✓
	Placement Density Analysis		✓	✓
	High-Speed rules based autorouting			✓
	Min/Max, matched length rules based autorouting			✓
	Pin-pair rules, Area rules based autorouting			✓
	Crosstalk controls, parallelism rules based autorouting			✓
	Differential Pair Autorouting, Automatic net shielding			✓
	High-speed rules-based autorouting			✓
	Layer-specific rules-based autorouting			✓
	256 signal layer limit			PCB Routing Option
	DFM rules-based autorouting			PCB Routing Option
	Automatic trace spreading			PCB Routing Option
	ATP generation			PCB Routing Option
	Layer-specific rules-based autorouting			PCB Routing Option
3.11	PSPICE SIMULATION	Orcad PCB Designer Standard	Orcad PCB Designer Professional	Allegro PCB Designer
	DC sweep, AC sweep, & transient analysis	Pspice AD	Pspice AD	Pspice AD
	Analog behavioural modelling	Pspice AD	Pspice AD	Pspice AD
	Stimulus editor	Pspice AD	Pspice AD	Pspice AD
	Model Editor for device characterization	Pspice AD	Pspice AD	Pspice AD
	Interactive waveform viewer & analyzer	Pspice AD	Pspice AD	Pspice AD
	Sensitivity: Identifies critical circuit components	Advanced Analysis	Advanced Analysis	Advanced Analysis
	Optimizer: Optimizes key circuit components	Advanced Analysis	Advanced Analysis	Advanced Analysis

	Monte Carlo: Analyzes statistical circuit behaviour and yield	Advanced Analysis	Advanced Analysis	Advanced Analysis
	Smoke: Detects component stress	Advanced Analysis	Advanced Analysis	Advanced Analysis
	Parametric Plotter: Examine solution through nested sweeps	Advanced Analysis	Advanced Analysis	Advanced Analysis
	PCB EDITOR	Orcad PCB Designer Standard	Orcad PCB Designer Professional	Allegro PCB Designer
	Physical and Spacing rules	✓	✓	✓
	Same net, Netclass, Class to Class rules	✓	✓	✓
	Pad Entry / Exit Rules	✓	✓	✓
6.16	Working Layer	✓	✓	✓
6.37	Constraint Manager adherence feedback (Red, Green, Yellow)	✓	✓	✓
	Floorplanning, Autoplace	✓	✓	✓
4.18	Group Route finish	✓	✓	✓
	Place by room / by schematic page	✓	✓	✓
3.37	Dynamic Shapes	✓	✓	✓
4.01	Snake Routing	✓	✓	✓
5.01	Push-n-Shove interactive editing	✓	✓	✓
	Curve Routing (Flex)	✓	✓	✓
3.27	Through Board Transparency	✓	✓	✓
4.18	Multi-line routing	✓	✓	✓
	Fan-out generators	✓	✓	✓
3.52	Flip Board	✓	✓	✓
	Dynamic pad suppression / Unused Pad removal	✓	✓	✓
	IDF 3.0 In/Out, DXF In/Out	✓	✓	✓
6.07	Native 3D viewer	✓	✓	✓
7.27	Gerber 274X, 274D artwork output	✓	✓	✓
7.27	Mentor® ODB++ and universal viewer	✓	✓	✓
	Design For Fabrication (DFF) Checks	✓	✓	✓
	Route cleanup, optimization (Glossing)	✓	✓	✓
	Silkscreen generation	✓	✓	✓
	Design For Test (DFT) / Test Prep	✓	✓	✓
	Soldermask, Solderpaste checks	✓	✓	✓
	Component height Checks	✓	✓	✓
5.18	Associative Dimensioning	✓	✓	✓
	Shape based Filleting		✓	✓
	Curved Fillet support		✓	✓
5.51	Placement replication, template based reuse		✓	✓
4.26	Differential Pairs rules and routing		✓	✓
4.07	Constraint Regions, region based rules (Rigid-Flex; BGA regions)		✓	✓
	Max Length		✓	✓
4.43	Interactive Delay Tuning		✓	✓
	Auto Test Prep		✓	✓
	Max Via Count			✓
	Dynamic Heads-up Display for critical rules			✓
	Dynamic DFA rules based interactive placement			✓
	Schematic based module reuse			✓
	Differential Pair Static Phase Control rules			✓
	Layer set rules			✓
	Extended (X)net rules			✓
	Estimated Crosstalk rules			✓
	Propagation delay rules (Min/Max, Relative)			✓
	Matched group rules			✓
	Pin Pair rules			✓
	T-Point rules (pin to T-point)			✓
5.35	Via array / Shielding			✓
	Design planning - Create hierarchical Bundles			✓
	Design planning - Create, Edit Flows			✓
	Design planning - Assign Flows to Layers			✓
	MCAD/ECAD Incremental design data exchange (EDMD)			✓
	Group route via pattern			✓
	Design Planning - Plan Spatial Feasibility analysis & feedback			Design Planning Option
	Design Planning - Generate Topological Plan			Design Planning Option
	Design Planning - Convert Topological plan to traces (CLINES)			Design Planning Option
	Design Planning - Plan Topological with Electrical rules			GRE Option
	Design Planning - Plan Accurate (final etch)			GRE Option
	Electrical Constraint rule set (ECSets) / Topology Apply			PCB High-Speed Option
	Electrical rules (Reflection, Timing, Crosstalk)			PCB High-Speed Option
	Package Pin Delay (for die-2-die delay) rules			PCB High-Speed Option
	Dynamic Differential Pair Phase Control rules			PCB High-Speed Option
	Z-Axis delay feedback			PCB High-Speed Option
	Extended Net creation			PCB High-Speed Option
	Advanced Constraints (formulas, relational)			PCB High-Speed Option
	Backdrilling			PCB High-Speed Option
	Segment over void detection			PCB High-Speed Option
	Spread lines between anti-pads			PCB High-Speed Option
	HDI Micro-via (spacing, stacking) rules			Miniaturization Option
	HDI micro-via inset (via-in-pad) rules			Miniaturization Option
	HDI micro-via stack editing			Miniaturization Option

	Orcad PCB Designer Standard	Orcad PCB Designer Professional	Allegro PCB Designer
Dynamic shape based filleting, line fattening and trace filleting			Miniaturization Option
Hug Contour routing (Flex)			Miniaturization Option
Single Click multiple micro- via instantiation			Miniaturization Option
Unused micro-via removal			Miniaturization Option
Manufacturing rule support for embedding components			Miniaturization Option
Embedded Packaged Components			Miniaturization Option
Support for Cavities on inner layers			Miniaturization Option
Concurrent Team Design - Layer by Layer			PCB Team Design Option
Concurrent Team Design - Functional block partitioning			PCB Team Design Option
Concurrent Team Design - Team design dashboard			PCB Team Design Option
Concurrent Team Design - Soft nets			PCB Team Design Option
Swap pins on a FPGA (based on FPGA rules) in PCB Editor			FPGA System Planner
Reoptimize pins on a FPGA (using FPGA rules)			FPGA System Planner
Parameterized RF etch elements			PCB Analog / RF Option
Asymmetrical Clearances			PCB Analog / RF Option
RF Etch elements editing			PCB Analog / RF Option
Bi-Directional interface with Agilent ADS			PCB Analog / RF Option
ADS schematics Import Agilent into DE-HDL			PCB Analog / RF Option
Layout-driven RF design creation			PCB Analog / RF Option
Flexible Shape Editor			PCB Analog / RF Option
Via Array placement on traces, shapes			PCB Analog / RF Option
E&OE			

To view our YouTube channel please go to www.youtube.com/parsyseda or scan the QR code

Time stamps refer to the **8 Minute Cadence PCB Suites and Options** video

