

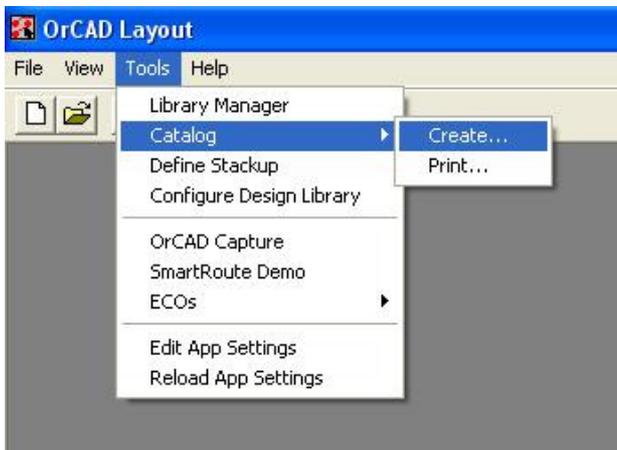


## Translating an Existing OrCAD Layout Library for use with PCB Editor

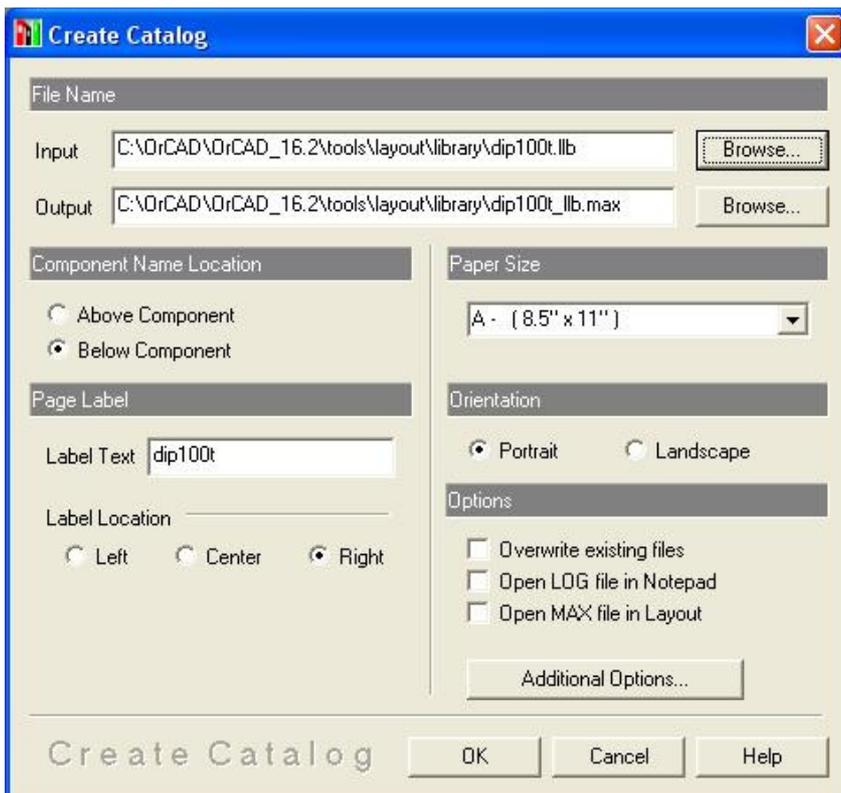
The OrCAD Layout to PCB Editor Translator translates OrCAD Layout design, MAX, files to PCB Editor BRD files. In order to translate an OrCAD Layout library, LLB, file for use with PCB Editor, the library must first be converted to a MAX file using the Catalog tool within OrCAD Layout. The resulting MAX file can then be translated with the Layout to PCB Editor Translator. The board file created can be modified with PCB Editor and the completed library parts exported for future use.

### Creating the Catalog

Start OrCAD Layout and, in the initial Layout Session window, use Tools>Catalog>Create from the menu.



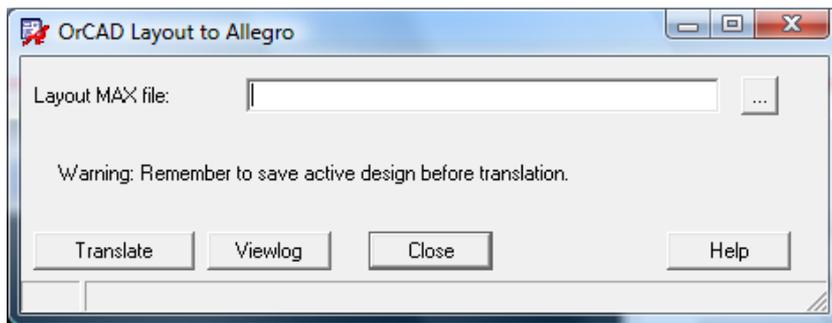
The Create Catalog dialog opens, use the upper Browse button to select the LLB file for translation.



(In this case one of the provided OrCAD Layout libraries is used as an example and the results written to the same directory, a better practice would be to take a copy of the LLB file to a working directory and process the data there.)

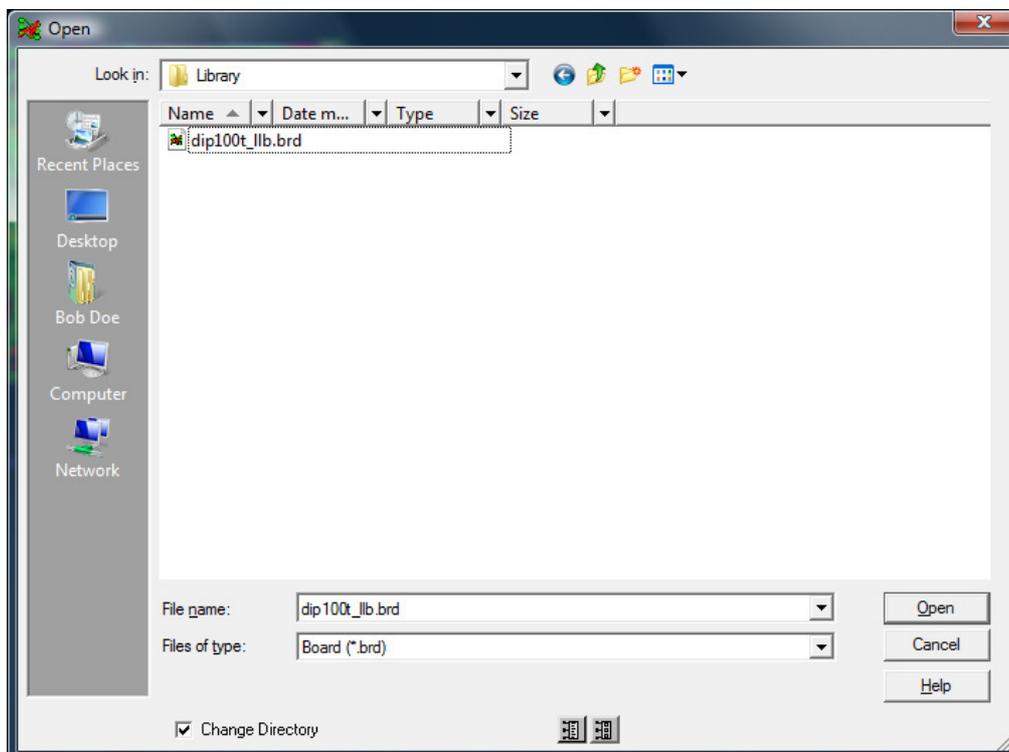
### Translating the Catalog file

Once the Catalog MAX file is created, the OrCAD Layout to PCB Editor translation can be run. Since the results will need review in PCB Editor, the translation will be run from there. Start PCB Editor, Start>Programs>Cadence>Release 16.5>OrCAD PCB Editor, then use File>Import>CAD Translators>OrCAD Layout.



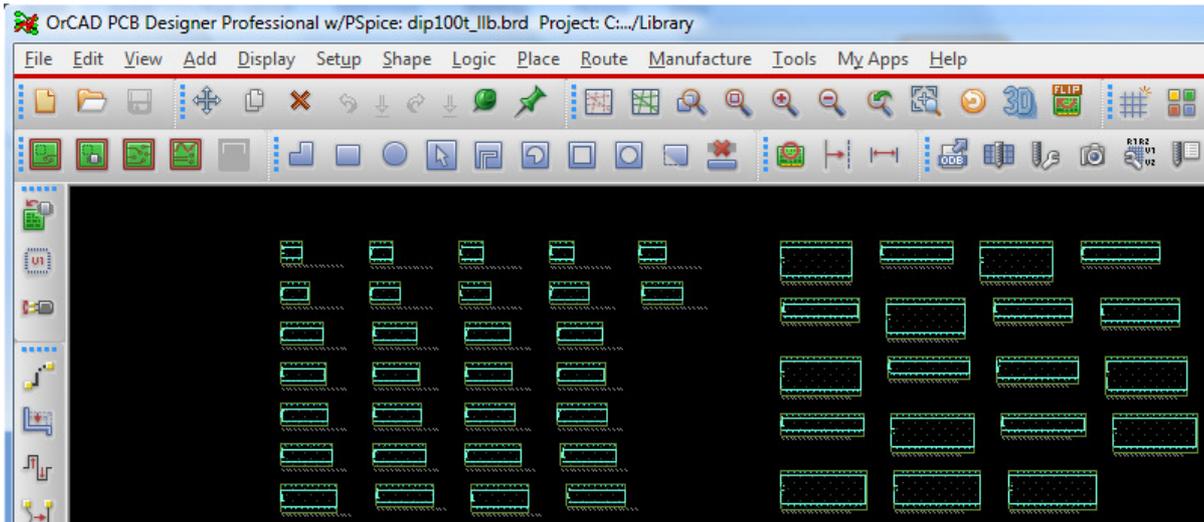
### Processing the data in PCB Editor

Browse to the MAX file just created from the Catalog tool and left-click on Translate to run the translation, the summary log file from the translation will be displayed. Left-click on Close to close the dialog and use File>Open, set the Files of Type to Board (BRD) and ensure that the Change Directory is checked.



Select the BRD file just created and left-click on Open, OK the warning that the DRC is invalid due to the change of tool, and the board file is opened in the PCB Editor canvas.

## Translating an Existing OrCAD Layout Library for use with PCB Editor



(Just a section of the screen is shown)

OrCAD Layout had two Inner Padstack Definitions in the library, one was for mapping to Plane layers and the other was for mapping to Inner layers. PCB Editor uses a single, “Default Inner” definition for all internal layers, whether Plane or Conductor, so the translated Plane and Inner Layers can be safely deleted from the stackup. From the menu, use Setup>Cross-Section to get the cross-section displayed.

Layout Cross Section

	Subclass Name	Type	Material	Thickness (MIL)	Conductivity (mho/cm)	Dielectric Constant
1		SURFACE	AIR			1
2	TOP	CONDUCTOR	COPPER	1.2	595900	4.5
3		DIELECTRIC	FR-4	8	0	4.5
4	PLANE	PLANE	COPPER	1.2	595900	4.5
5		DIELECTRIC	FR-4	8	0	4.5
6	INNER	CONDUCTOR	COPPER	1.2	595900	4.5
7		DIELECTRIC	FR-4	8	0	4.5
8	BOTTOM	CONDUCTOR	COPPER	1.2	595900	4.5
9		SURFACE	AIR			1

Move the mouse to the “PLANE” subclass and right-click>Remove Layer to remove the layer.

Layout Cross Section

	Subclass Name	Type	Material	Thickness (MIL)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent
1		SURFACE	AIR			1	0
2	TOP	CONDUCTOR	COPPER	1.2	595900	4.5	0
3		DIELECTRIC	FR-4	8	0	4.5	0.035
4	PI	CONDUCTOR	COPPER	1.2	595900	4.5	0
5		DIELECTRIC	FR-4	8	0	4.5	0.035
6	IN	CONDUCTOR	COPPER	1.2	595900	4.5	0
7		DIELECTRIC	FR-4	8	0	4.5	0.035
8	BOTTOM	CONDUCTOR	COPPER	1.2	595900	4.5	0
9		SURFACE	AIR			1	0

Context menu options for row 4 (PI):

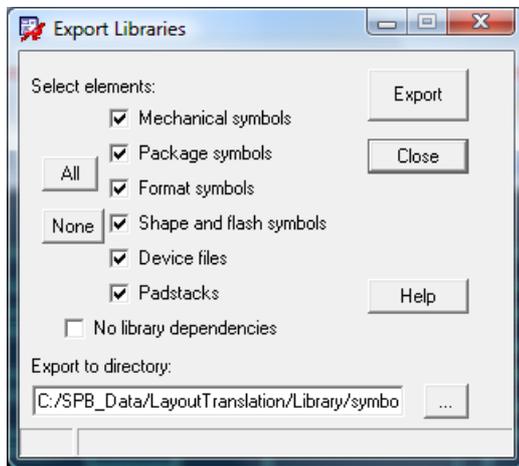
- Add Layer Above
- Add Layer Below
- Remove Layer

Repeat the Remove Layer steps for the “INNER” and redundant DIELECTRIC layers.

	Subclass Name	Type	Material	Thickness (MIL)	Conductivity (mho/cm)	Dielectric Constant
1		SURFACE	AIR			1
2	TOP	CONDUCTOR	COPPER	1.2	595900	4.5
3		DIELECTRIC	FR-4	8	0	4.5
4	BOTTOM	CONDUCTOR	COPPER	1.2	595900	4.5
5		SURFACE	AIR			1

OK to close the Cross-section editor and save the board in this state, File>Save.

Then use File>Export>Libraries, leave all the “boxes” checked. The libraries will be exported to the current directory but it might be preferable to create a new directory to specifically store the exported data since a number of files will typically be created. The example below sent the data to a symbols directory in the current directory.



Left-click on Export to run the process. Any errors will be reported to the displayed log file, if there are no errors, the log file will not be displayed.

The exported data will be in the form of DRA files which are the symbol sources. PSM files which are the compiled symbols actually used by PCB Editor, and PAD files which contain the padstack definitions.

The exported symbols should be opened with PCB Editor as a final check. Since Layout allowed the use of internally named padstacks, it might be preferable to check and revise the padstack names to something more descriptive than the default internal names from the source data.

To use the symbols, move the DRA and PSM files to the library source folder, set this in the PSMPATH User Preference for PCB Editor and either, move the PAD files to the same directory, or use a specific location to hold the PAD files. Be sure to specify this location in the PADPATH User Preference.

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