

Introduction

A differential pair is a pair of conductors used for differential signalling. Differential pairs are usually found on a printed circuit board, in cables (twisted-pair cables, ribbon cables), and in connectors. The term can also refer to a pair of transistors used as the input stage of a differential amplifier. By using this technique minimises crosstalk and electromagnetic interference, both noise emission and noise acceptance, and can achieve a constant and/or known characteristic impedance, allowing impedance matching techniques is important in a high-speed signal transmission line or high quality balanced line and balanced circuit audio signal path. This technical note covers: -

- Auto Generation of Diff Pair Objects
- Grouping Diff Pairs with Net Classes
- Driving rules with the Physical CSET including Min Line Space and Tolerance
- Region support for Diff Pair Line Width and Gap
- Setting up Electrical Rules (Uncoupling, Phase, Relative Delay)

How to Define Differential Pairs.

It should be noted that since 17.2 any level of the Cadence PCB Tools can generate differential pairs but for certain rules you may need to use a different license (Dynamic Phase for example).

We start by defining the differential pairs in the design. Just to note differential pairs can be setup in the schematic (Tools – Create – Differential Pairs in OrCAD Capture) and are defined in Constraint Manager when imported via a netlist or they can be setup manually using Setup>Constraints>Constraint Manager (or Setup>Constraints in OrCAD) which launches Constraint Manager. Select the Electrical>Net>Routing>Differential Pair folder then use Objects>Create>Differential Pair. Select Auto Setup. The following GUI will appear: -

🗖 Differential P	air Automatic Setup				?×
Net	~	Prefix: DP_	+ Filter: P	- Filter: N	
All Nets ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 ADDR5 ADDR6 ADDR6 ADDR7 ADDR8 ADDR9 ADDR9 ADDR10 A1	Diff Pair	Diff Pair DP_PECL1_ DP_PECL2_ DP_PHASE_	+ Net PECL1_P PECL2_P PHASE_P	-Net PECL1_N PECL2_N PHASE_N	
Filter:		Create	Remove	Close	Help

For this example I have used Prefix = DP_; + filter = P; - filter = N. Nets with a common root name with suffixes P and N will be listed. Select Create then Close the remaining forms. This is used to sort through the net names and locate your differential pairs. Use suitable prefixes and filters for your design.

Click on the Physical domain>Net>All Layers Workbook noting the newly created Diff Pair (DPr) Objects.

Electrical		_	Objecto	Deferrend	Line	Width
+ Physical			Objects	Physical CSet	Min	Max
🖃 🛅 Physical Constraint Set	Туре	S	Name		mil	mil
All Layers	*	*	χ.	*	*	*
🖻 🛅 Net	Dsn		 diffpairs 	DEFAULT	5.00	0.00
All Layers	ОТур		🛨 Buses			
Region	ОТур		Diff Pairs			
	DPr		DP_PECL1_	DEFAULT	5.00	0.00
An cayers	DPr			DEFAULT	5.00	0.00
	DPr		DP_PHASE_	DEFAULT	5.00	0.00
	ОТур		+ XNets/Nets			

Now Create a Net Class for the Diff Pairs. With the LMB (left mouse button) select/drag the 3 Diff Pair Objects then RMB (right mouse button) Create>Class. For this example the name of DP_CLASS is used. This step can also take place in the Spacing Domain. Net Classes allow us to apply constraints at the top of the hierarchy. Net Classes will be used to create spacing rules between the DP_CLASS and will also be used in a Region application later in this note.

🗲 Electrical					Line To ≫	Thru Pin To >>	SMD Pin To >>	Test Pin To ≫	Thru \
+ Physical			Objects	Referenced	All	All	All	All	
Spacing	Туре	S	Name	spacing coer	mil	mil	mil	mil	r
E-E Spacing Constraint Set	*	*	*	*	*	*	*	*	*
All Layers	Dsn		diffpairs	DEFAULT	4.00	***	4.00	4.00	4.00
Net	ОТур		Net Classes						
	NCIs		DP_CLASS (3)	DEFAULT	4.00	***	4.00	4.00	4.00
	DPr		DP_PECL1_	DEFAULT	4.00	***	4.00	4.00	4.00
Net Class-Class	Net		PECL1_N	DEFAULT	4.00	***	4.00	4.00	4.00
III All Layers	Net	Π	PECL1_P	DEFAULT	4.00	***	4.00	4.00	4.00
CSet assignment matrix	DPr	Π	DP_PECL2_	DEFAULT	4.00	***	4.00	4.00	4.00
🖕 庙 Region	Net		PECL2_N	DEFAULT	4.00	***	4.00	4.00	4.00
All Layers	Net		PECL2_P	DEFAULT	4.00	***	4.00	4.00	4.00
- Inter Laver	DPr		DP_PHASE_	DEFAULT	4.00	***	4.00	4.00	4.00
	ОТур		🕂 Buses						
······ ··· - 5	ОТур		XNets/Nets						

Next we define the Diff Pair Physical Rules. Under Physical domain>Physical Constraint Set>All Layers create a new Physical CSet called DP100. To do this Click on the Default CSet then RMB>Create>Physical CSet. Enter the name DP100 then add the following values for the DP100 rule. You will need to expand the + next the DP100 name to enter the alternate layer rules.

- a. Min Line Width 8 mil for outer layers, 6 mil for inner layers.
- b. Primary Gap 8 mil for outer layers, 6 mil for inner layers.
- c. +/- Tolerance 0.2 mil on outer layers, 0.1 mil for inner layers.
- d. Min Line Space 7.8 mil for outer layers, 5.9 mil for inner layers.

diffp	airs											
		Objects	Peferenced	Line	Width	Ne	ck			Differential Pair	r	
		objecta	Physical CSet	Min	Max	Min Width	Max Length	Min Line Spaci	Primary Gap	Neck Gap	(+)Tolerance	(-)Tolerance
Туре	S	Name		mil	mil	mil	mil	mil	mil	mil	mil	mil
*	*	ż	*	*	*	*	*	*	*	*	*	*
Dsn		 diffpairs 	DEFAULT	5.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PCS		DEFAULT		5.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PCS		DP100		8.00:6.00:6	0.00	0.00	0.00	7.80:5.90:5	8.00:6.00:6	0.00	0.20:0.10:0	0.20:0.10:0
LTyp		Conductor		6.00	0.00	0.00	0.00	5.90	6.00	0.00	0.10	0.10
Lyr	1	TOP		8.00	0.00	0.00	0.00	7.80	8.00	0.00	0.20	0.20
Lyr	2	SIGNAL_2		6.00	0.00	0.00	0.00	5.90	6.00	0.00	0.10	0.10
Lyr	3	SIGNAL_3		6.00	0.00	0.00	0.00	5.90	6.00	0.00	0.10	0.10
Lyr	4	SIGNAL_4		6.00	0.00	0.00	0.00	5.90	6.00	0.00	0.10	0.10
Lyr	5	SIGNAL_5		6.00	0.00	0.00	0.00	5.90	6.00	0.00	0.10	0.10
Lyr	6	SIGNAL_6		6.00	0.00	0.00	0.00	5.90	6.00	0.00	0.10	0.10
Lyr	7	SIGNAL_7		6.00	0.00	0.00	0.00	5.90	6.00	0.00	0.10	0.10
Lyr	8	BOTTOM		8.00	0.00	0.00	0.00	7.80	8.00	0.00	0.20	0.20

Note on Min Line Space and Tolerance - Use primary or neck gap, whatever is lower minus the negative tolerance value. In the above example: -

Min line space (outers) = 8.0 - .2 = 7.8 Min line space (inners) = 6.0 - .1 = 5.9

A Min Line Space DRC is reported if the Diff Pair Gap is below 7.8 outers and 5.9 inners. If the Min Line Space is left blank, the Diff Pair Gap will be derived from the line to line spacing rule used in the Spacing domain. The following two figures show a graphical representation of the basic settings for a differential pair.



Now apply the new Physical CSet to the Net Class DP_CLASS. Click on Net>All Layers workbook in the Physical Domain and Click on the Referenced Physical CSet cell adjacent to the DP_CLASS and select DP100 from the drop-down list.

How to define Differential Pairs

Worksheet Selector	₽×	diffpa	airs	•]		
Æ Electrical						Line
+ft Physical				Objects	Referenced Physical C Set	Min
Physical Constraint Set		Туре	S	Name	- Thysical coct	mil
All Layers		*	*	*	*	*
⊨ line internet inte		Dsn		 diffpairs 	DEFAULT	5.00
All Lavers		ОТур		Net Classes		
Region		NCIs		DP_CLASS (3)	DP100	8.00:6.00:6.00
		DPr		DP_PECL1_	DP100	8.00:6.00:6.00
All Layers		DPr		DP_PECL2_	DP100	8.00:6.00:6.00
		DPr		DP_PHASE_	DP100	8.00:6.00:6.00
		ОТур		🕂 Buses		
		ОТур		Diff Pairs		
		ОТур		+ XNets/Nets		

Differential Pairs can be defined as an Electrical CSet or a Physical CSet. You can define Min Line Spacing, Primary Gap, Primary Width, Neck Gap, Neck Width, + and – Tolerance as either a Physical or Electrical CSet. The differences being that if you wish to change the track thickness and spacing as the differential pair changes layers in the PCB to control impedance then they should be defined as a Physical CSet. If the track thickness and gap remains the same throughout the cross section of the PCB then it is recommended that the differential pair be defined as an Electrical CSet. This is also true if you wish to use Constraint Regions to control a different set of design rules by area e.g. smaller track and gap widths. For Constraint Regions the differential pairs MUST be defined as a Physical CSet. Uncoupled length and phase (static and dynamic must be defined as an Electrical CSet so you may find you have both an Electrical CSet and a Physical CSet to control the differential pairs. You will see the values for Min Line Spacing, Primary Gap, Primary Width, Neck Gap, Neck Width, + and – Tolerance will be inherited from the Physical / Electrical domains depending on how they are defined.

As part of designs that use BGA's PCB Editor (Allegro or OrCAD Professional) gives users the option to define a Constraint Region around the BGA then have a different set of design rules that control that area e.g. smaller track and gap widths. To do this in the PCB Editor main window (you can leave the Constraint Manager window open). Zoom into the area where the BGA's are located, for this example we are going to add a Constraint Region Shape to the bottom side of the board. Use Shape>Rectangular, from the Options menu set the class / subclass to Constraint Region / Bottom. Enter a Region name of BGA in the Assign to Region field, then draw a rectangle around the BGA using either the LMB or the RMB>Snap Pick to function.



Once the Region has been defined, open Constraint Manager and Click on the Region>All Layers Workbook in the Physical Domain. We wish to use the Region to control just the differential pair line width and gap, not all signals that cut across it. This is best solved by the use of a "Region Class" Constraint object. Select the BGA Region then use RMB>Create>Region-Class.

Flectrical			Ohiosta		Lin	e Width	h		N	eck						Diff
🖡 Physical			Objects	Physical CSet	Min		Max	Mir	n Width	Max	Length	Min L	ine Spaci	Prim	ary Gap	
🗐 🛅 Physical Constraint Set	Туре	S	Name		mil		mil		mil		mil		mil		mil	
All Layers	*	* *		*	*	*		*		*		*		*		*
🛅 Net	Dsn		diffpairs	DEFAULT	5.00	0.00	<u> </u>	0.00	<u> </u>	0.00		0.00	<u> </u>	0.00	<u> </u>	0.0
All Layers	Rgn		BGA													
				Create Re	gioriciasses											
All Layers				🎢 Create Re	gionClasses										?	×
				Regions:					Net	Classes:						
				BGA					DP	_CLASS						

From the popup GUI, select the Net Class DP_Class then click OK.

Worksheet Selector	₽×	diffpa	airs]			
F Electrical				Ohiosta		Line	Width
+ Physical				Objects	Physical C Set	Min	Max
🖃 🔚 Physical Constraint Set		Туре	S	Name		mil	mil
All Layers		*	* :	ż	*	*	*
⊡ • internet		Dsn		- diffpairs	DEFAULT	5.00	0.00
All Layers		Rgn		- BGA			
		RCIs		DP_CLASS			
All Layers							

The "Region-Class" (RCls) is slightly indented from the "Region" object BGA. The constraints assigned to the "Region-Class" take precedence over constraints assigned to the "Region" object (BGA).

There are now two options to consider:

How to define Differential Pairs

- i. Create and assign a Physical CSet to the "Region-Class"
- ii. Directly set values (also called an override)

We will directly set the values on the basis of there are only 3 constraints involved and no variance is required across layers. Enter 3.5 mil for Min Line Width, 4 mil for Primary Gap and 3.8 for Min Line Spacing (4.0 Region Gap - 0.2 Tolerance). Click NO to any assertion message that may appear when entering in values for gap and min line space.

Worksheet Selector & X	diffp	airs													
🗲 Electrical			Ohiasta			Line	Width	1	N	eck	Т				Diffe
+f+ Physical			Objects	Physical C Set		Min		Мах	Min Width	Max Length	Min L	ine Spaci	Primar	y Gap	Ne
🖃 🛅 Physical Constraint Set	Туре	S	Name			mil		mil	mil	mil		mil	m	il	
All Layers	*	* *		*	*		*		*	*	*		*		*
📄 🛅 Net	Dsn	ΠE	diffpairs	DEFAULT	5.00	******	0.00	*****	0.00	0.00	0.00	*****	0.00	*****	0.00
All Lavers	Rgn		BGA												
Region	RCIs		DP_CLASS		3.50						3.80		4.00		
All Layers															

DP100_12

F

Next we are going to define the Diff Pair general Spacing Rules. The following figure represents the spacing rules required for this example between Diff Pairs and other nets. Diff Pairs are required to be spaced at 10 mils to each other and 12 mils to other nets. The Primary Gap was set in the previous steps. See the Physical Constraint setup above.



We start by creating a new Spacing CSet called DP100_10; Click on the Default CSet then RMB>Create>Spacing CSet. Enter name DP100_10. Change the Line to Line space to 10 mils. Now create another Spacing CSet called DP100_12. Change Line to Line space to 12 mils. The figure below shows the Spacing CSets defined.

diffpa	airs _.	_17.2								
		Objects	Deferenced						Line To <<	
		Objecta	Spacing CSet	All	Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via
Туре	S	Name	opuonig ooot	mil	mil	mil	mil	mil	mil	mil
	*	*	*	*	*	*	*	*	*	*
sn		diffpairs_17.2	DEFAULT	4.00	4.00	4.00	4.00	4.00	4.00	4.00
CS		DEFAULT		4.00	4.00	4.00	4.00	4.00	4.00	4.00
CS		E DP100 10		***	10.00	4 00	4 00	4 00	4 00	4 00

Assign the Spacing CSet DP100_12 to the Net Class DP_CLASS. This rule sets a 12 mil line to line space from the Diff Pair objects to all other nets.

4.00

4.00

4.00

4.00

12.00

Worksheet Selector	₽×	diffpa	irs	_17.2						
Electrical				Objects					Li	in
+ Physical				Objects	Referenced Spacing CSet	All	Line	Thru Pin	SMD Pin	ſ
🖵 Spacing		Туре	S	Name		mil	mil	mil	mil	ſ
Spacing Constraint Set		*	*	*	*	*	*	*	*	*
All Layers		Dsn		diffpairs_17.2	DEFAULT	4.00	4.00	4.00	4.00	2
n in Net		ОТур		Net Classes						
		NCIs		DP_CLASS (3)	DP100_12	***	12.00	4.00	4.00	4
		DPr			DP100_12	***	12.00	4.00	4.00	4
		DPr		DP_PECL2_	DP100_12	***	12.00	4.00	4.00	4
All Layers		DPr		DP_PHASE_	DP100_12	***	12.00	4.00	4.00	4
CSet assignment matrix		ОТур		🕂 Buses						
E Egion		ОТур		XNets/Nets						

Now create a Net Class-Class object. A "Net Class-Class" object (NCC) is used to control line spacing between Net Classes; both inter and intra relationships. Click on the Net Class-Class - All layers workbook. Click on the Net Class

Test Via

mil

4.00

4.00

4.00

4.00

4.00

Shape

mil

4 00

4.00

4.00

4.00

DP_CLASS then RMB>Create>Class-Class. Click Apply or OK to create the relationship that is presented in the GUI shown below.



Assign the CSET DP100_10 to the NCC object as shown below.

Worksheet !	Selector	₽×	diffpa	aira	s_17.2			
4	Electrical			_			Line To ≫	Thru I
+[+	Physical				Objects	Referenced Spacing C Set	All	
I	Spacing		Туре	S	Name	opacing coor	mil	
🖃 🕒 Sp	acing Constraint Set		*	*	*	*	*	*
Ī	All Lavers		Dsn		diffpairs_17.2	DEFAULT	4.00	***
📄 🛅 Ne	t		NCIs		DP_CLASS (1)	DP100_12	***	***
	All Lavers		CCIs		DP_CLASS	DP100_10 🗸	***	***
e 🕒 Ne	et Class-Class All Layers CSet assignment matrix							

Now we need to define the Electrical Rule Setup (Uncoupling and Phase Control). Click on the Electrical Domain – Electrical Constraint Set – Diff Pair Worksheet. Create an Electrical CSet called DP100. Enter Gather Control = Ignore; Uncoupled Max Length = 300 mil and Static Phase Tolerance = 25 mil. Leave all other cells blank as we are using the Physical CSET to drive these rules. If values are entered in the Electrical CSET, they will take precedence over rules set from a Physical CSET.

Worksheet Se	lector 🗗 🗙	diff	pair	s_17	.2					
4	Electrical				Objects	Uncoupled	I Length	Static Phase	Min Line	
🖃 🛅 Elect	rical Constraint Set				objects	Cathon Control	Max	Tolerance	Spacing	Prima
📄 👘 R	outing	Тур	2 9	5	Name	Gather Control	mil	mil	mil	n
	Wiring	*	*	*		*	*	*	*	*
	Impedance	Dsn	Т	Þ	diffpairs_17.2				0.00	0.00
	Min/Max Propagation Delays	ECS			DP100	Ignore	300.00	25 mil		
	Total Etch Length									
	Differential Pair									
🖮 📔 Net										

Apply the ECSET DP100 to the Diff Pairs. Click on the Net – Diff Pair Worksheet and Apply the ECSet DP100 to the 3 Diff Pairs.

🗲 Electrical	Objecto				Sta						
🖃 🛅 Electrical Constraint Set		Objects		Referenced	Gather	Length Ignore	Max	Actual	Margin	Tolerance	
🖮 🖣 Routing	Туре	S	Name		Control	mil	mil	mil	mil	mil	
···· 🖩 Wiring	*	*	*	*	*	*	*	*	*	*	
Impedance	Dsn		diffpairs_17.2								
Min/Max Propagation Delays	ОТур		🕂 Buses								
Total Etch Length	ОТур		Diff Pairs								
Differential Pair	DPr		DP_PECL1_	DP100 🗸	Ignore		300.00			25 mil	
n Net	DPr			DP100	Ignore		300.00			25 mil	
🖞 📠 Routing	DPr		DP_PHASE_	DP100	Ignore		300.00			25 mil	
I Wing	ОТур		XNets/Nets								
wing											
Min/Max Propagation Delays											
Total Etch Length											
Differential Pair											
🔢 Differential Pair											

Electrical Rule Setup

Cadence OrCAD PCB Designer Professional and Allegro PCB Designer

Using an Electrical Rule Setup (Matched Group). Click on the Net – Relative Propagation Delay Worksheet. Expand each of the 3 Diff Pairs to see their net members then select each net with the LMB. Use the Control key to extend the selection. Once the 6 nets are selected, use the RMB>Create>Matched Group command then for this example enter a name of DP_MATCH. Working on the Matched Group row, enter Pin Pairs = Longest Pin Pair, Scope = Global and Delta:tolerance = 0:25.

Worksheet Selector 🗗 🗙	diffp	airs	_17.2							
🖗 Electrical	Objects		Defensed.			Relative Delay				
🖃 🛅 Electrical Constraint Set		Objects		Flectrical C Set	Pin Pairs	Scope	Delta:Tolerance	Antical	Manufin	
🗄 📲 Routing	Туре	S	Name	Libernearedet			mil	Actual	margin	
🖃 🛅 Net	*	*	*	*	*	*	*	*	*	
Routing	Dsn		diffpairs_17.2							
Wiring	ОТур		Match Groups							
Impedance	MGrp		DP_MATCH (6)		Longest Pin Pair	Global	0 mil:25 mil		\sim	
Min/Max Propagation Delays	Net		PECL1_N	DP100	Longest Pin Pair	Global	0 mil:25 mil	$\sim\sim\sim\sim\sim$		
Total Etch Longth	Net		PECL1_P	DP100	Longest Pin Pair	Global	0 mil:25 mil	******	~~~~~	
	Net		PECL2_N	DP100	Longest Pin Pair	Global	0 mil:25 mil		******	
	Net		PECL2_P	DP100	Longest Pin Pair	Global	0 mil:25 mil	******	******	
Relative Propagation Delay	Net		PHA SE_N	DP100	Longest Pin Pair	Global	0 mil:25 mil	\sim	~~~~~	
	Net	П	PHA SE_P	DP100	Longest Pin Pair	Global	0 mil:25 mil	******	*******	

Since the Diff Pairs are not routed, the Actual and Margin cells appear in Yellow. DRC results based on actual unrouted lengths can be produced by setting the Unrouted Relative Delay DRC followed by an update of the DRC system. To enable the DRC from Constraint Manager, go to Analyze>Analysis Modes>Electrical, then enable the "Relative propagation delay in the DRC unrouted section. Constraint Manager will now show the match group updated with green and red bars. A Target is automatically assigned to the member of the group with the longest Manhattan length. The setup is now complete. You can route the differential pairs, get real time feedback whilst routing to meet the constraints defined.

Flectrical	Objects					Relat		Lawath	Delau		
🖃 🛅 Electrical Constraint Set		Objects	Electrical C Set	Pin Pairs	Scope	Delta:Tolerance	A			Length	Delay
🞰 🖣 Routing	Туре	S Name	Lioutitui ouot			mil	Actual	wargin	+/-	mil	ns
🖃 📲 Net	*	* *	*	*	*	*	*	*	*	*	*
E Routing	Dsn	diffpairs_17.2						468.03 mil			
Wiring	ОТур	Match Groups									
Impedance	MGrp	DP_MATCH (6)		Longest Pin Pair	Global	0 mil:25 mil		468.03 mil			
Min/Max Propagation Delays	Net	PECL1_N	DP100	Longest Pin Pair	Global	0 mil:25 mil		83.22 mil			
Total Etch Length	RePP	U6.Y13:U11.10			Global	0 mil:25 mil	108.22 mil	83.22 mil	888	1122.41	0.21568
Differential Daia	Net	PECL1_P	DP100	Longest Pin Pair	Global	0 mil:25 mil		6.15 mil			
	RePP	U6.Y14:U11.9			Global	0 mil:25 mil	18.85 mil	6.15 mil	883	1211.78	0.23174
Relative Propagation Delay	Net	PECL2_N	DP100	Longest Pin Pair	Global	0 mil:25 mil		468.03 mil			
	RePP	U6.W6:U11.13			Global	0 mil:25 mil	493.03 mil	468.03 mil	888	737.60	0.14642
	Net	PECL2_P	DP100	Longest Pin Pair	Global	0 mil:25 mil		457.4 mil			
	RePP	U6.W5:U11.12			Global	0 mil:25 mil	482.4 mil	457.4 mil	888	748.23	0.14833
	Net	PHASE_N	DP100	Longest Pin Pair	Global	0 mil:25 mil		39.97 mil			
	RePP	U6.E7:U12.3			Global	0 mil:25 mil	64.97 mil	39.97 mil	888	1165.66	0.21575
	Net	PHASE_P	DP100	Longest Pin Pair	Global	0 mil:25 mil					
	RePP	U6.E8:U12.2			Global	0 mil:25 mil	TARGET		~~~	1230.63	0.22742
	OTvn	E Bucoc								(

Adding Impedance Rules

Many differential pairs also require to be routed to a specific width to meet an impedance based rule. OrCAD PCB Designer Professional and Allegro PCB Designer level licenses and above are able to do this. To add an impedance rule open Constraint Manager – Electrical – Electrical Constraint Set – Routing – Impedance and either create a new electrical Cset (ECS) or define the impedance and tolerance (either as a % or ohm) to an existing rule.

How to define Differer	ntial Pairs												
				orkshee	t Selector	X di	iffoair	17.2					
				ş	Electrical		in pui		1	Sir	ale line l	mnedan	
)- 🛅 E	lectrical Constraint Set			Objects	Referenced	Target	Toleran	Actual	Margin
				ė-¶	Routing	Ту	pe S	Name	Electrical C Set	Ohm	Ohm	Ohm	Ohm
					🎟 Wiring	*	*	*	*	*	*	*	•
						Dsn	1	diffpairs_17.2					*****
					- III Min/Max Propagation Delay	s OTy	/P	🛨 Buses					
Worksheet Selector 🗗 🗙	diffpairs 17.2				🖩 Total Etch Length	ОТу	/P	Diff Pairs					
4 Electrical	· -			- '	Differential Pair	DPr			DP100	100	2%		
Electrical Constraint Set	Objects	Single-line	Impedance	_)-🗀 N	let	Net		PECL1_N DECL1_D	DP100	100	2 %		
		Target	Tolerance	- i-Q	Routing	DPr			DP100	100	2%		
	Type S Name	Ohm	Ohm	_	III Wiring	Net		PECL2 N	DP100	100	2 %		
····· Wiring	<u> </u>	1	*	_		Net		PECL2_P	DP100	100	2 %		
Impedance	Dsn _ diffpairs_17.2				- III Min/Max Propagation Delay	s DPr		DP_PHASE_	DP100	100	2 %		
Min/Max Propagation Delays	ECS DP100	100	2 %	_	Total Etch Length	Net		PHA SE_N	DP100	100	2 %		×****
Total Etch Length					Differential Pair	Net		PHASE_P	DP100	100	2 %		
Differential Pair					🖩 Relative Propagation Delay	ОТу	/p						

Once defined, the rules can be applied to the Nets – Impedance area of Constraint Manager as shown above right. You can now begin to route the differential pair. You will notice that because you have applied an impedance rule to the nets that the routing function behaves slightly differently because as you route PCB Editor invokes a 2D field solver to analyse the route thickness to ensure it meets the rules defined. Other points to note when using impedance based rules are that the Cross Section of the PCB **MUST** be defined accurately. The material, thickness, conductivity, dielectric constant and loss tangent can all affect the impedance rule. You **MUST** also define a suitable Shield layer. There are also options to setup Single and Differential Impedances or use the differential impedance calculator (Allegro PCB Designer only). Refer to the cmug.pdf located at <your_install_dir>\doc\cmug\ for further details.

💱 Differential Calculator									
Layer name: TOP	•								
Differential impedance:	92.748 ohm 💿								
Single-line impedance:	60.724 ohm								
Line width:	0.250 MM 💿								
Primary gap:	0.130 MM 💿								
Select a button to choose a recalculation target.									
Close	Help								

Note: - Many users of Impedance based traces often talk directly to the PCB Fabricator to confirm or indeed define the actual width of the trace that requires to be of a certain impedance. This is largely down to the fact that PCB substrates often vary in performance and construction, pre-preg's used can also differ, all which have a huge effect on the actual impedance of a trace. Fabricators are responsible for manufacturing your finished PCB's so if they define the impedance trace width they often use tools based on their current stock material. If you prefer to use this flow, the MIN_LINE_WIDTH can be defined with this information meaning that you do not need to set up the impedance rules. Using a physical constraint rule will usually result in a much better routing performance since the 2D solver will not be running during the routing process.

Appendix

Note: - for Phase Tuning you need either an Allegro PCB Designer or OrCAD Professional license (or higher). For Dynamic Phase settings you require an Allegro PCB Designer license (or higher).

Dynamic Phase Control for Differential Pairs



Differential Pair (Diff Pair) technology has evolved where more stringent checking is required in the area of phase control. This is evident on higher data rates associated with parallel buses such as QPI, SMI, PCI Gen 2, DDR, QDR and Infiniband. In the simplest of terms, Diff Pair technology is sending opposite and equal signals down a pair of traces. Keeping these opposite signals in phase is essential in assuring that they function as intended.

The Dynamic Phase check is designed to meet the guidelines that suggest that the path lengths of the true and complement signals within the differential pair must differ by no more than "x mils" along the entire path of the net. If at any point on the net, the skew between true and complement exceeds "x mils", this mismatch needs to be compensated within "y mils". Representative values for x and y might be x = 20 and y = 600.

The constraints associated with Differential Pairs support Static and Dynamic Phase. The margins of each constraint can be set independently using length or time. The Max Length (running skew) constraint for Dynamic Phase is limited to

length only.

Static Phase Tolerance – a one-time check from Driver to Receiver comparing lengths or delay of each member. If a Driver cannot be determined, the check is performed across the longest path of the pair.

Dynamic Phase – Etch length of each member is compared at each bend point interval across the Driver-Receiver path of the Diff Pair. Etch length is always measured back to the Driver pins.

Dynamic Phase Max Length – When specified, the Diff Pair is permitted to exceed the phase tolerance constraint for a contiguous etch length of less than or equal to the value of Max Length specified. If no compensation is made within this specified distance, a DRC will be reported at the point where the Diff Pair first goes out of phase.

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🖃 🛅 Electrical Constraint Set		Objects -		Cathor Control		Max		Tolerance		Max Length	Toler	ance		
🖮 ᆒ Routing	Туре	S	Na	me		Gauler Co	muor	m	il	mil		mil	m	il
Wiring	*	* *				*		*		*		*	*	
···· 🖽 Vias	Dsn	LE	diffpairs	_17.2										
Impedance	ECS		DP100		[Include	\sim	300.00		25 mil		600.00	20 mil	
Min/Max Propagation Delays														
🖩 🛛 Total Etch Length														
📰 Differential Pair														
🖩 Relative Propagation Delay														

As an example, suppose your Dynamic Phase constraints are set as follows:

Static Phase	Dynamic Phase							
Tolerance	Max Length	Tolerance						
mil	mil	mil						
*	*	*	*					
			0.					
20 mil	300.00	20 mil	1					

When the DRC is updated, it shows the following:



The beginning of the yellow pseudo line (closest to driver) is where the Diff Pair initially goes out of Phase (beyond the 20 mil Static Phase tolerance). The DRC marker *D*-*Y* is placed at the initial 'out of phase spec' location as measured from the Driver Pins.

Notes:

- There can only be 1 DRC marker on a pair, even though there may be multiple violation zones.
- It is assumed that the designer will correct the phase issues working from the Drivers to the Receivers.

Differential Phase Tuning

Phase Tuning is an alternative to using the mouse guided delay tune command and offers the precision of finite length adjustment to differential signals that are length/phase constrained. It is especially effective on static or dynamic phase-constrained Differential Pairs where iterative etch compensation may be required at various points along the path of either member of the pair. Simply make a mouse click at any point on the cline path to add in a single-parameterized phase bump.

The command is located in the Route Menu of the PCB Editor. When invoked, parameters can be set in the Options panel. Select a style of Line or Arc then define its respective length/size parameters. The form will compute the added compensation for each bump before applying you it.

How to define Differential Pairs





Phase Tune Options

Differential Phase Bumps

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