Introduction

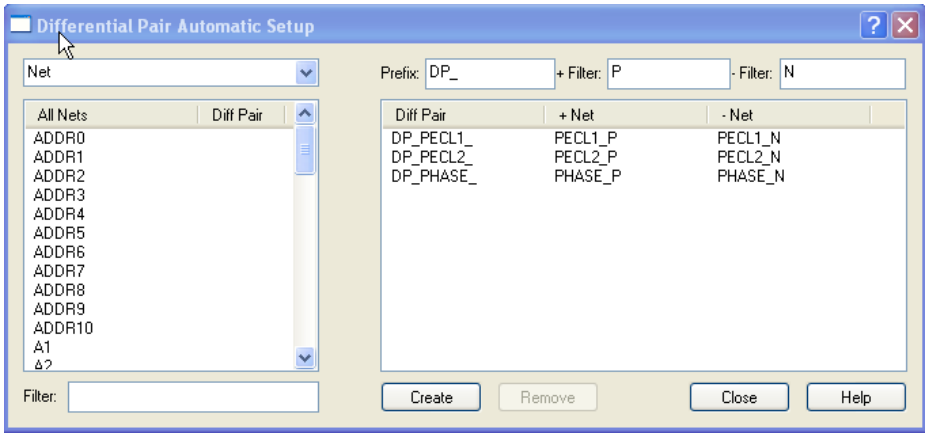
A differential pair is a pair of conductors used for differential signalling. Differential pairs are usually found on a printed circuit board, in cables (twisted-pair cables, ribbon cables), and in connectors. The term can also refer to a pair of transistors used as the input stage of a differential amplifier. By using this technique minimises crosstalk and electromagnetic interference, both noise emission and noise acceptance, and can achieve a constant and/or known characteristic impedance, allowing impedance matching techniques is important in a high-speed signal transmission line or high quality balanced line and balanced circuit audio signal path. This technical note covers: -

- Auto Generation of Diff Pair Objects
- Grouping Diff Pairs with Net Classes
- Driving rules with the Physical CSET including Min Line Space and Tolerance
- Region support for Diff Pair Line Width and Gap
- Setting up Electrical Rules (Uncoupling, Phase, Relative Delay)

How to Define Differential Pairs.

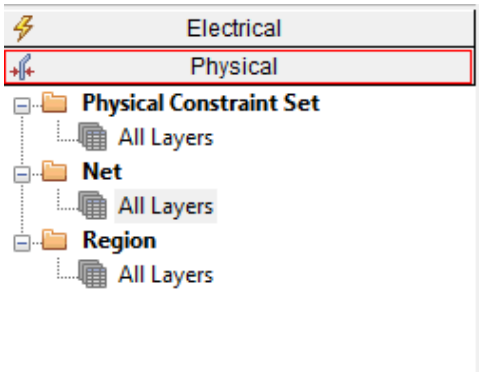
It should be noted that since 17.2 any level of the Cadence PCB Tools can generate differential pairs but for certain rules you may need to use a different license (Dynamic Phase for example).

We start by defining the differential pairs in the design. Just to note differential pairs can be setup in the schematic (Tools – Create – Differential Pairs in OrCAD Capture) and are defined in Constraint Manager when imported via a netlist or they can be setup manually using Setup>Constraints>Constraint Manager (or Setup>Constraints in OrCAD) which launches Constraint Manager. Select the Electrical>Net>Routing>Differential Pair folder then use Objects>Create>Differential Pair. Select Auto Setup. The following GUI will appear: -



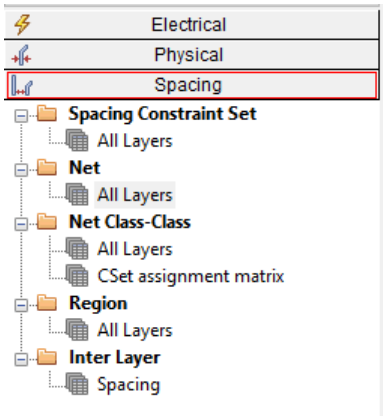
For this example I have used Prefix = DP_; + filter = P; - filter = N. Nets with a common root name with suffixes P and N will be listed. Select Create then Close the remaining forms. This is used to sort through the net names and locate your differential pairs. Use suitable prefixes and filters for your design.

Click on the Physical domain>Net>All Layers Workbook noting the newly created Diff Pair (DPr) Objects.



Objects			Referenced Physical CSet	Line Width	
				Min	Max
Type	S	Name		mil	mil
*	*	*	*	*	*
Dsn		⊟ diffpairs	DEFAULT	5.00	0.00
OTyp		⊞ Buses			
OTyp		⊟ Diff Pairs			
DPr		⊞ DP_PECL1_	DEFAULT	5.00	0.00
DPr		⊞ DP_PECL2_	DEFAULT	5.00	0.00
DPr		⊞ DP_PHASE_	DEFAULT	5.00	0.00
OTyp		⊞ XNets/Nets			

Now Create a Net Class for the Diff Pairs. With the LMB (left mouse button) select/drag the 3 Diff Pair Objects then RMB (right mouse button) Create>Class. For this example the name of DP_CLASS is used. This step can also take place in the Spacing Domain. Net Classes allow us to apply constraints at the top of the hierarchy. Net Classes will be used to create spacing rules between the DP_CLASS and will also be used in a Region application later in this note.



Objects			Referenced Spacing CSet	Line To >>	Thru Pin To >>	SMD Pin To >>	Test Pin To >>	Thru V
				All	All	All	All	
Type	S	Name		mil	mil	mil	mil	r
*	*	*	*	*	*	*	*	*
Dsn		⊟ diffpairs	DEFAULT	4.00	***	4.00	4.00	4.00
OTyp		⊟ Net Classes						
NCls		⊟ DP_CLASS (3)	DEFAULT	4.00	***	4.00	4.00	4.00
DPr		⊟ DP_PECL1_	DEFAULT	4.00	***	4.00	4.00	4.00
Net		PECL1_N	DEFAULT	4.00	***	4.00	4.00	4.00
Net		PECL1_P	DEFAULT	4.00	***	4.00	4.00	4.00
DPr		⊟ DP_PECL2_	DEFAULT	4.00	***	4.00	4.00	4.00
Net		PECL2_N	DEFAULT	4.00	***	4.00	4.00	4.00
Net		PECL2_P	DEFAULT	4.00	***	4.00	4.00	4.00
DPr		⊞ DP_PHASE_	DEFAULT	4.00	***	4.00	4.00	4.00
OTyp		⊞ Buses						
OTyp		⊞ XNets/Nets						

Next we define the Diff Pair Physical Rules. Under Physical domain>Physical Constraint Set>All Layers create a new Physical CSet called DP100. To do this Click on the Default CSet then RMB>Create>Physical CSet. Enter the name DP100 then add the following values for the DP100 rule. You will need to expand the + next the DP100 name to enter the alternate layer rules.

a. Min Line Width 8 mil for outer layers, 6 mil for inner layers.
b. Primary Gap 8 mil for outer layers, 6 mil for inner layers.
c. +/- Tolerance 0.2 mil on outer layers, 0.1 mil for inner layers.
d. Min Line Space 7.8 mil for outer layers, 5.9 mil for inner layers.

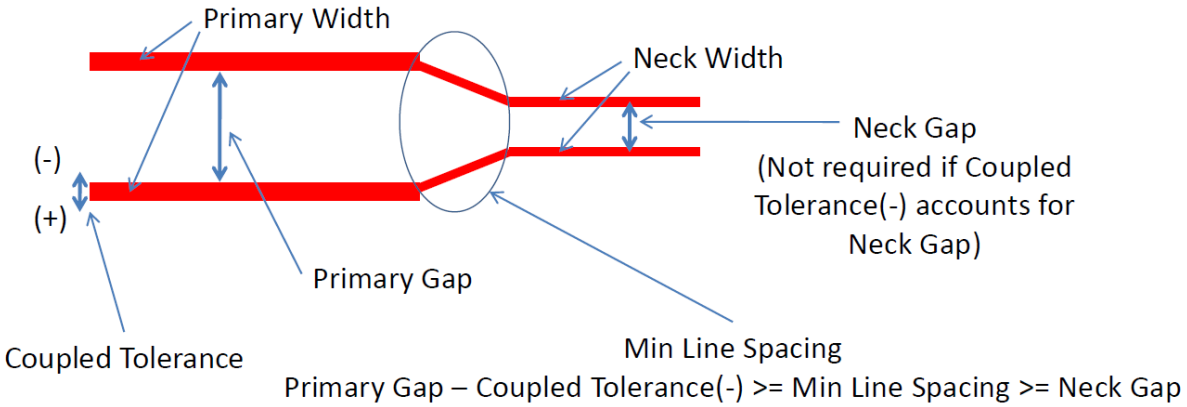
diffpairs

Objects			Referenced Physical CSet	Line Width		Neck		Differential Pair				
				Min	Max	Min Width	Max Length	Min Line Spaci	Primary Gap	Neck Gap	(+)Tolerance	(-)Tolerance
Type	S	Name		mil	mil	mil	mil	mil	mil	mil	mil	mil
*	*	*	*	*	*	*	*	*	*	*	*	*
Dsn		⊟ diffpairs	DEFAULT	5.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PCS		⊞ DEFAULT		5.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
PCS		⊟ DP100		8.00:6.00:6....	0.00	0.00	0.00	7.80:5.90:5....	8.00:6.00:6....	0.00	0.20:0.10:0....	0.20:0.10:0....
LTyp		⊟ Conductor		6.00	0.00	0.00	0.00	5.90	6.00	0.00	0.10	0.10
Lyr	1	TOP		8.00	0.00	0.00	0.00	7.80	8.00	0.00	0.20	0.20
Lyr	2	SIGNAL_2		6.00	0.00	0.00	0.00	5.90	6.00	0.00	0.10	0.10
Lyr	3	SIGNAL_3		6.00	0.00	0.00	0.00	5.90	6.00	0.00	0.10	0.10
Lyr	4	SIGNAL_4		6.00	0.00	0.00	0.00	5.90	6.00	0.00	0.10	0.10
Lyr	5	SIGNAL_5		6.00	0.00	0.00	0.00	5.90	6.00	0.00	0.10	0.10
Lyr	6	SIGNAL_6		6.00	0.00	0.00	0.00	5.90	6.00	0.00	0.10	0.10
Lyr	7	SIGNAL_7		6.00	0.00	0.00	0.00	5.90	6.00	0.00	0.10	0.10
Lyr	8	BOTTOM		8.00	0.00	0.00	0.00	7.80	8.00	0.00	0.20	0.20

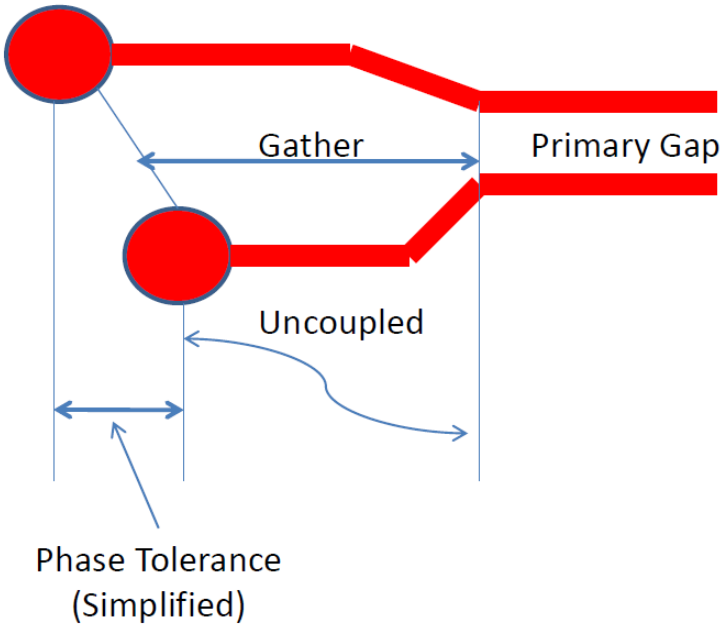
Note on Min Line Space and Tolerance - Use primary or neck gap, whatever is lower minus the negative tolerance value. In the above example: -

Min line space (outers) = 8.0 - .2 = 7.8
Min line space (inners) = 6.0 - .1 = 5.9

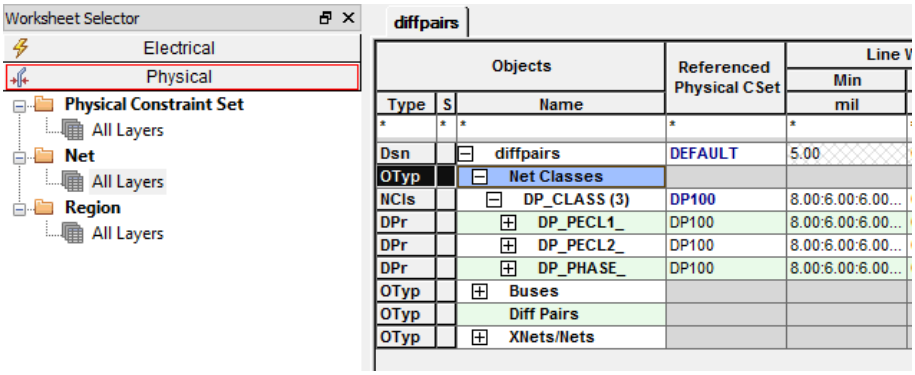
A Min Line Space DRC is reported if the Diff Pair Gap is below 7.8 outers and 5.9 inners. If the Min Line Space is left blank, the Diff Pair Gap will be derived from the line to line spacing rule used in the Spacing domain. The following two figures show a graphical representation of the basic settings for a differential pair.



Pair is Uncoupled
IF (Gap < Primary Gap – Coupled Tolerance(-))
OR (Gap > Primary Gap + Coupled Tolerance(+))
OR (Gap < Neck Gap)

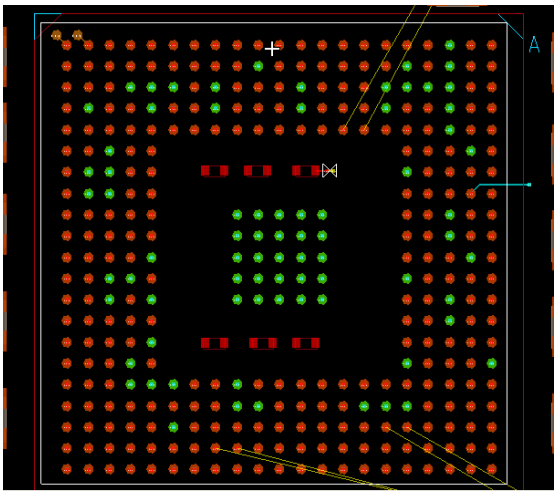


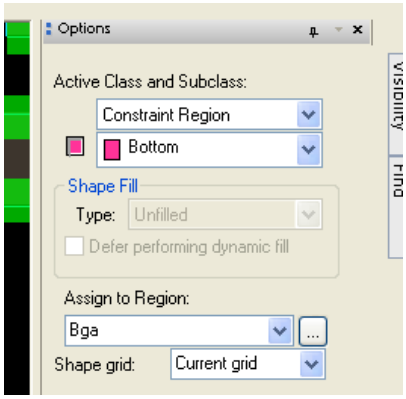
Now apply the new Physical CSet to the Net Class DP_CLASS. Click on Net>All Layers workbook in the Physical Domain and Click on the Referenced Physical CSet cell adjacent to the DP_CLASS and select DP100 from the drop-down list.



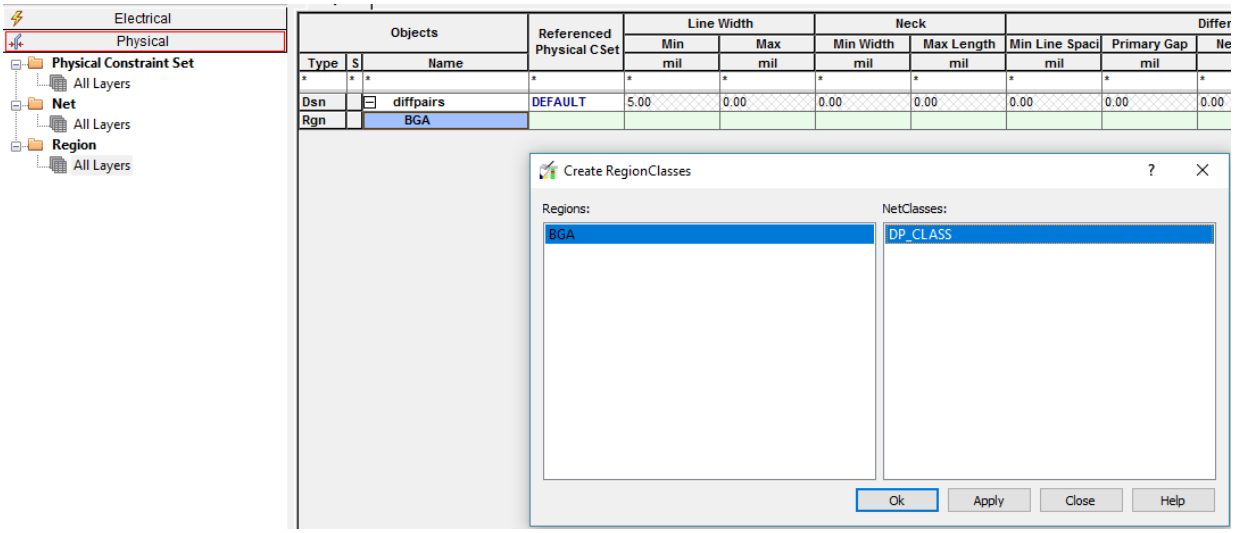
Differential Pairs can be defined as an Electrical CSet or a Physical CSet. You can define Min Line Spacing, Primary Gap, Primary Width, Neck Gap, Neck Width, + and – Tolerance as either a Physical or Electrical CSet. The differences being that if you wish to change the track thickness and spacing as the differential pair changes layers in the PCB to control impedance then they should be defined as a Physical CSet. If the track thickness and gap remains the same throughout the cross section of the PCB then it is recommended that the differential pair be defined as an Electrical CSet. This is also true if you wish to use Constraint Regions to control a different set of design rules by area e.g. smaller track and gap widths. For Constraint Regions the differential pairs MUST be defined as a Physical CSet. Uncoupled length and phase (static and dynamic must be defined as an Electrical CSet so you may find you have both an Electrical CSet and a Physical CSet to control the differential pairs. You will see the values for Min Line Spacing, Primary Gap, Primary Width, Neck Gap, Neck Width, + and – Tolerance will be inherited from the Physical / Electrical domains depending on how they are defined.

As part of designs that use BGA's PCB Editor (Allegro or OrCAD Professional) gives users the option to define a Constraint Region around the BGA then have a different set of design rules that control that area e.g. smaller track and gap widths. To do this in the PCB Editor main window (you can leave the Constraint Manager window open). Zoom into the area where the BGA's are located, for this example we are going to add a Constraint Region Shape to the bottom side of the board. Use Shape>Rectangular, from the Options menu set the class / subclass to Constraint Region / Bottom. Enter a Region name of BGA in the Assign to Region field, then draw a rectangle around the BGA using either the LMB or the RMB>Snap Pick to function.

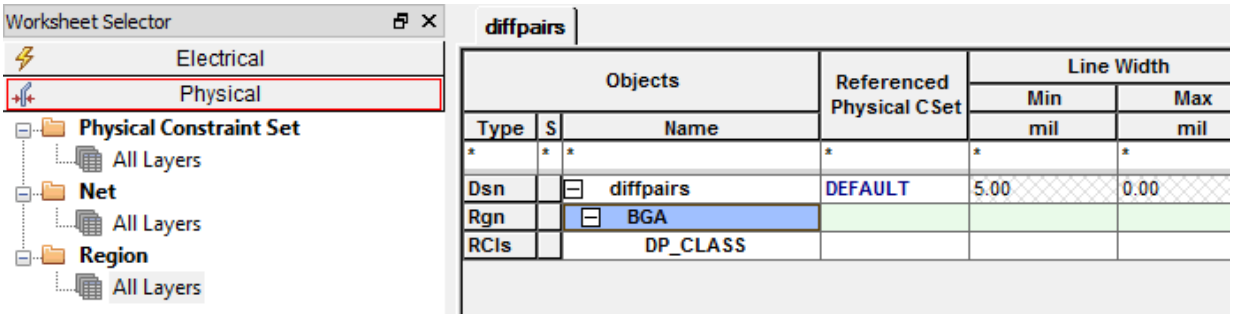




Once the Region has been defined, open Constraint Manager and Click on the Region>All Layers Workbook in the Physical Domain. We wish to use the Region to control just the differential pair line width and gap, not all signals that cut across it. This is best solved by the use of a "Region Class" Constraint object. Select the BGA Region then use RMB>Create>Region-Class.



From the popup GUI, select the Net Class DP_Class then click OK.



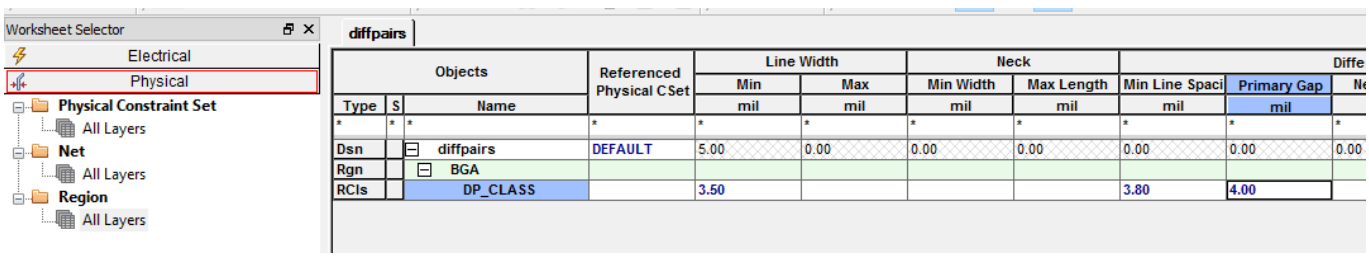
The “Region-Class” (RCls) is slightly indented from the “Region” object BGA. The constraints assigned to the “Region-Class” take precedence over constraints assigned to the “Region” object (BGA).

There are now two options to consider:

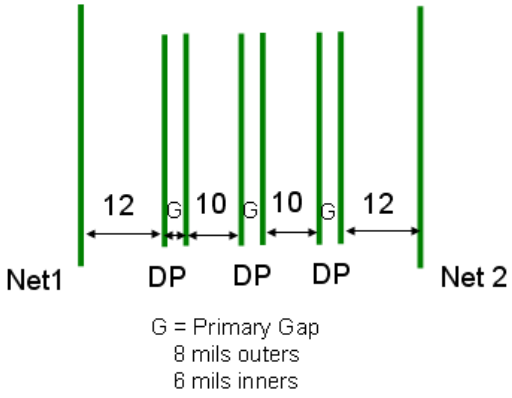
i. Create and assign a Physical CSet to the “Region-Class”

ii. Directly set values (also called an override)

We will directly set the values on the basis of there are only 3 constraints involved and no variance is required across layers. Enter 3.5 mil for Min Line Width, 4 mil for Primary Gap and 3.8 for Min Line Spacing (4.0 Region Gap - 0.2 Tolerance). Click NO to any assertion message that may appear when entering in values for gap and min line space.



Next we are going to define the Diff Pair general Spacing Rules. The following figure represents the spacing rules required for this example between Diff Pairs and other nets. Diff Pairs are required to be spaced at 10 mils to each other and 12 mils to other nets. The Primary Gap was set in the previous steps. See the Physical Constraint setup above.

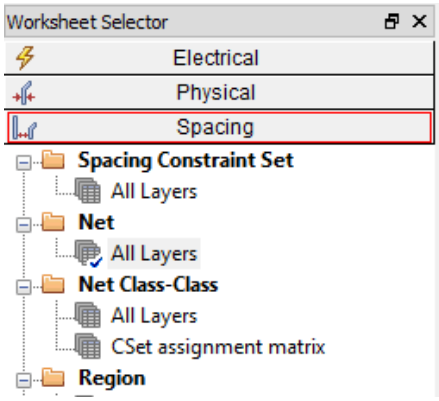


We start by creating a new Spacing CSet called DP100_10; Click on the Default CSet then RMB>Create>Spacing CSet. Enter name DP100_10. Change the Line to Line space to 10 mils. Now create another Spacing CSet called DP100_12. Change Line to Line space to 12 mils. The figure below shows the Spacing CSets defined.

diffpairs_17.2

Objects			Referenced Spacing CSet	Line To <<								
				All	Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Shape
Type	S	Name		mil	mil	mil	mil	mil	mil	mil	mil	mil
*	*	*	*	*	*	*	*	*	*	*	*	*
Dsn		⊟ diffpairs_17.2	DEFAULT	4.00	4.00	4.00	4.00	4.00	4.00	4.00	4.00	4.00
SCS		⊞ DEFAULT		4.00	4.00	4.00	4.00	4.00	4.00	4.00	4.00	4.00
SCS		⊞ DP100_10		***	10.00	4.00	4.00	4.00	4.00	4.00	4.00	4.00
SCS		⊞ DP100_12		***	12.00	4.00	4.00	4.00	4.00	4.00	4.00	4.00

Assign the Spacing CSet DP100_12 to the Net Class DP_CLASS. This rule sets a 12 mil line to line space from the Diff Pair objects to all other nets.

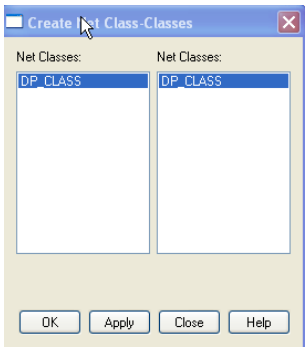


diffpairs_17.2

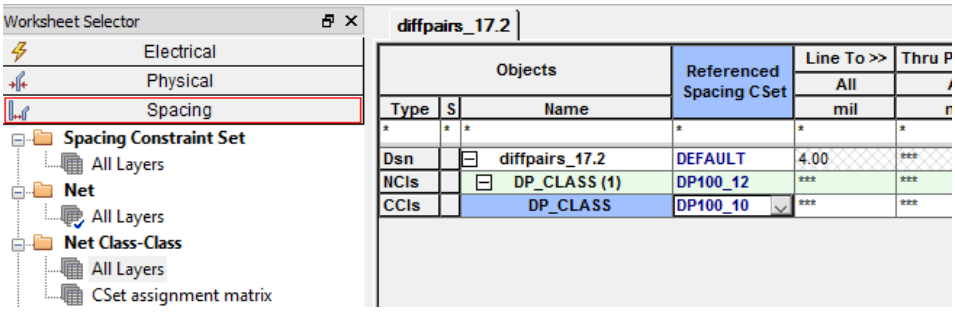
Objects			Referenced Spacing CSet	All	Line	Thru Pin	SMD Pin
Type	S	Name		mil	mil	mil	mil
*	*	*	*	*	*	*	*
Dsn		⊟ diffpairs_17.2	DEFAULT	4.00	4.00	4.00	4.00
OTyp		⊟ Net Classes					
NCls		⊟ DP_CLASS (3)	DP100_12	***	12.00	4.00	4.00
DPr		⊞ DP_PECL1_	DP100_12	***	12.00	4.00	4.00
DPr		⊞ DP_PECL2_	DP100_12	***	12.00	4.00	4.00
DPr		⊞ DP_PHASE_	DP100_12	***	12.00	4.00	4.00
OTyp		⊞ Buses					
OTyp		⊞ XNets/Nets					

Now create a Net Class-Class object. A “Net Class-Class” object (NCC) is used to control line spacing between Net Classes; both inter and intra relationships. Click on the Net Class-Class - All layers workbook. Click on the Net Class

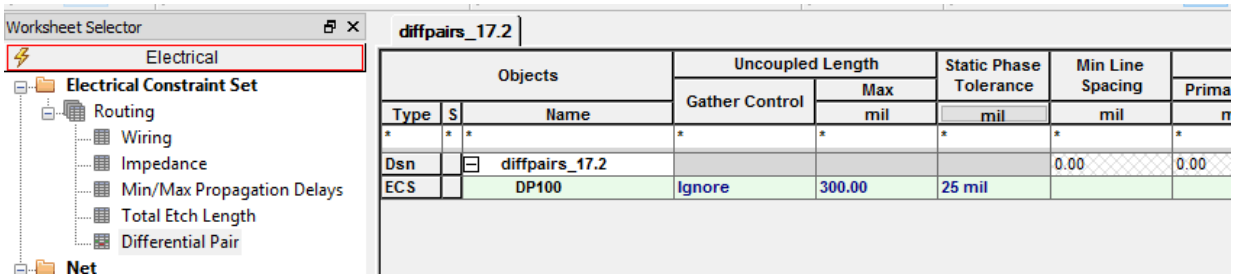
DP_CLASS then RMB>Create>Class-Class. Click Apply or OK to create the relationship that is presented in the GUI shown below.



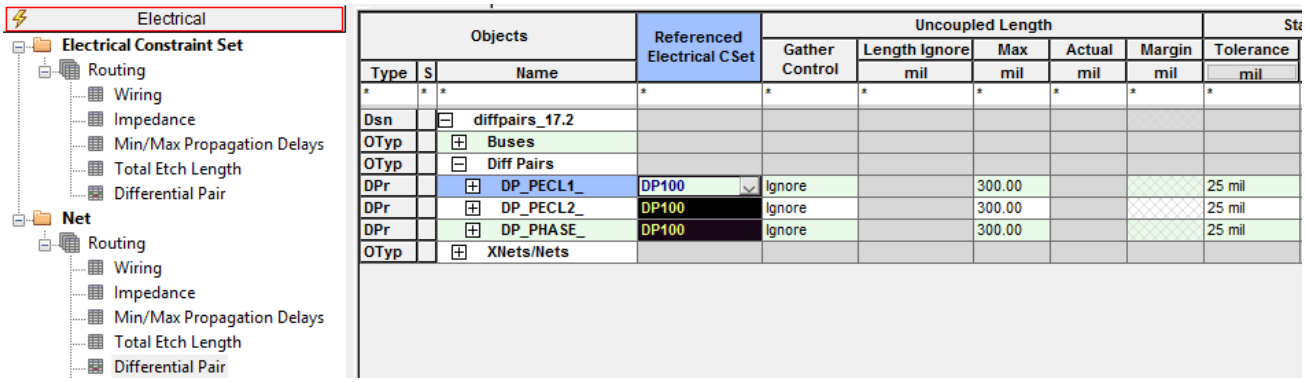
Assign the CSET DP100_10 to the NCC object as shown below.



Now we need to define the Electrical Rule Setup (Uncoupling and Phase Control). Click on the Electrical Domain – Electrical Constraint Set – Diff Pair Worksheet. Create an Electrical CSet called DP100. Enter Gather Control = Ignore; Uncoupled Max Length = 300 mil and Static Phase Tolerance = 25 mil. Leave all other cells blank as we are using the Physical CSET to drive these rules. If values are entered in the Electrical CSET, they will take precedence over rules set from a Physical CSET.



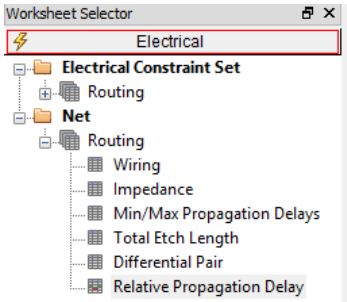
Apply the ECSET DP100 to the Diff Pairs. Click on the Net – Diff Pair Worksheet and Apply the ECSet DP100 to the 3 Diff Pairs.



Electrical Rule Setup

Cadence OrCAD PCB Designer Professional and Allegro PCB Designer

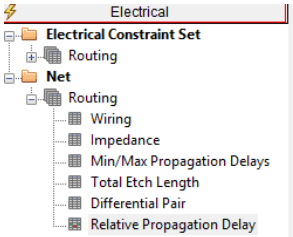
Using an Electrical Rule Setup (Matched Group). Click on the Net – Relative Propagation Delay Worksheet. Expand each of the 3 Diff Pairs to see their net members then select each net with the LMB. Use the Control key to extend the selection. Once the 6 nets are selected, use the RMB>Create>Matched Group command then for this example enter a name of DP_MATCH. Working on the Matched Group row, enter Pin Pairs = Longest Pin Pair, Scope = Global and Delta:tolerance = 0:25.



diffpairs_17.2

Objects			Referenced Electrical CSet	Pin Pairs	Scope	Relative Delay		
Type	S	Name				Delta:Tolerance mil	Actual	Margin
*	*	*	*	*	*	*	*	*
Dsn		diffpairs_17.2						
OTyp		Match Groups						
MGrp		DP_MATCH (6)		Longest Pin Pair	Global	0 mil:25 mil		
Net		PECL1_N	DP100	Longest Pin Pair	Global	0 mil:25 mil		
Net		PECL1_P	DP100	Longest Pin Pair	Global	0 mil:25 mil		
Net		PECL2_N	DP100	Longest Pin Pair	Global	0 mil:25 mil		
Net		PECL2_P	DP100	Longest Pin Pair	Global	0 mil:25 mil		
Net		PHASE_N	DP100	Longest Pin Pair	Global	0 mil:25 mil		
Net		PHASE_P	DP100	Longest Pin Pair	Global	0 mil:25 mil		

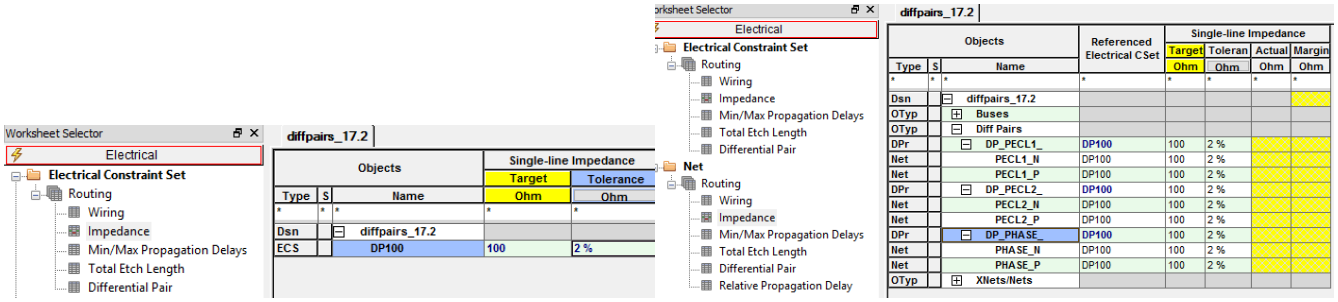
Since the Diff Pairs are not routed, the Actual and Margin cells appear in Yellow. DRC results based on actual unrouted lengths can be produced by setting the Unrouted Relative Delay DRC followed by an update of the DRC system. To enable the DRC from Constraint Manager, go to Analyze>Analysis Modes>Electrical, then enable the "Relative propagation delay in the DRC unrouted section. Constraint Manager will now show the match group updated with green and red bars. A Target is automatically assigned to the member of the group with the longest Manhattan length. The setup is now complete. You can route the differential pairs, get real time feedback whilst routing to meet the constraints defined.



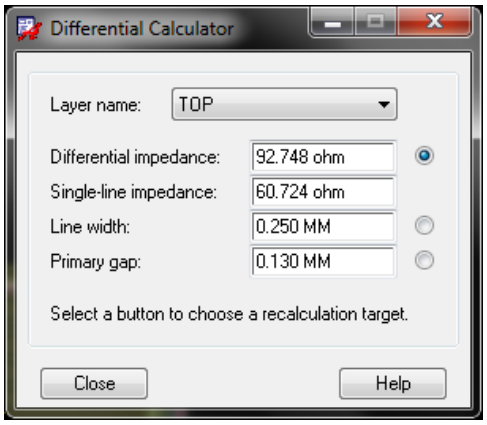
Objects			Referenced Electrical CSet	Pin Pairs	Scope	Relative Delay				Length	Delay
Type	S	Name				Delta:Tolerance mil	Actual	Margin	+/-	mil	ns
*	*	*	*	*	*	*	*	*	*	*	*
Dsn		diffpairs_17.2						468.03 mil			
OTyp		Match Groups									
MGrp		DP_MATCH (6)		Longest Pin Pair	Global	0 mil:25 mil		468.03 mil			
Net		PECL1_N	DP100	Longest Pin Pair	Global	0 mil:25 mil		83.22 mil			
RePP		U6.Y13:U11.10			Global	0 mil:25 mil	108.22 mil	83.22 mil	-	1122.41	0.21568
Net		PECL1_P	DP100	Longest Pin Pair	Global	0 mil:25 mil		6.15 mil			
RePP		U6.Y14:U11.9			Global	0 mil:25 mil	18.85 mil	6.15 mil	-	1211.78	0.23174
Net		PECL2_N	DP100	Longest Pin Pair	Global	0 mil:25 mil		468.03 mil			
RePP		U6.W6:U11.13			Global	0 mil:25 mil	493.03 mil	468.03 mil	-	737.60	0.14642
Net		PECL2_P	DP100	Longest Pin Pair	Global	0 mil:25 mil		457.4 mil			
RePP		U6.W5:U11.12			Global	0 mil:25 mil	482.4 mil	457.4 mil	-	748.23	0.14833
Net		PHASE_N	DP100	Longest Pin Pair	Global	0 mil:25 mil		39.97 mil			
RePP		U6.E7:U12.3			Global	0 mil:25 mil	64.97 mil	39.97 mil	-	1165.66	0.21575
Net		PHASE_P	DP100	Longest Pin Pair	Global	0 mil:25 mil					
RePP		U6.E8:U12.2			Global	0 mil:25 mil	TARGET			1230.63	0.22742
OTyp		Buses									

Adding Impedance Rules

Many differential pairs also require to be routed to a specific width to meet an impedance based rule. OrCAD PCB Designer Professional and Allegro PCB Designer level licenses and above are able to do this. To add an impedance rule open Constraint Manager – Electrical – Electrical Constraint Set – Routing – Impedance and either create a new electrical Cset (ECS) or define the impedance and tolerance (either as a % or ohm) to an existing rule.



Once defined, the rules can be applied to the Nets – Impedance area of Constraint Manager as shown above right. You can now begin to route the differential pair. You will notice that because you have applied an impedance rule to the nets that the routing function behaves slightly differently because as you route PCB Editor invokes a 2D field solver to analyse the route thickness to ensure it meets the rules defined. Other points to note when using impedance based rules are that the Cross Section of the PCB **MUST** be defined accurately. The material, thickness, conductivity, dielectric constant and loss tangent can all affect the impedance rule. You **MUST** also define a suitable Shield layer. There are also options to setup Single and Differential Impedances or use the differential impedance calculator (Allegro PCB Designer only). Refer to the cmug.pdf located at <your_install_dir>\doc\cmug\ for further details.

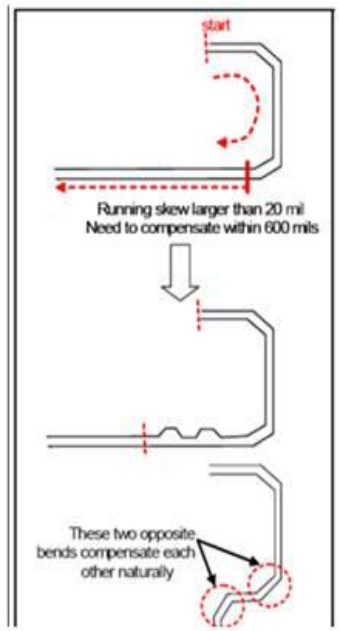


Note: - Many users of Impedance based traces often talk directly to the PCB Fabricator to confirm or indeed define the actual width of the trace that requires to be of a certain impedance. This is largely down to the fact that PCB substrates often vary in performance and construction, pre-preg's used can also differ, all which have a huge effect on the actual impedance of a trace. Fabricators are responsible for manufacturing your finished PCB's so if they define the impedance trace width they often use tools based on their current stock material. If you prefer to use this flow, the MIN_LINE_WIDTH can be defined with this information meaning that you do not need to set up the impedance rules. Using a physical constraint rule will usually result in a much better routing performance since the 2D solver will not be running during the routing process.

Appendix

Note: - for Phase Tuning you need either an Allegro PCB Designer or OrCAD Professional license (or higher). For Dynamic Phase settings you require an Allegro PCB Designer license (or higher).

Dynamic Phase Control for Differential Pairs



Differential Pair (Diff Pair) technology has evolved where more stringent checking is required in the area of phase control. This is evident on higher data rates associated with parallel buses such as QPI, SMI, PCI Gen 2, DDR, QDR and Infiniband. In the simplest of terms, Diff Pair technology is sending opposite and equal signals down a pair of traces. Keeping these opposite signals in phase is essential in assuring that they function as intended.

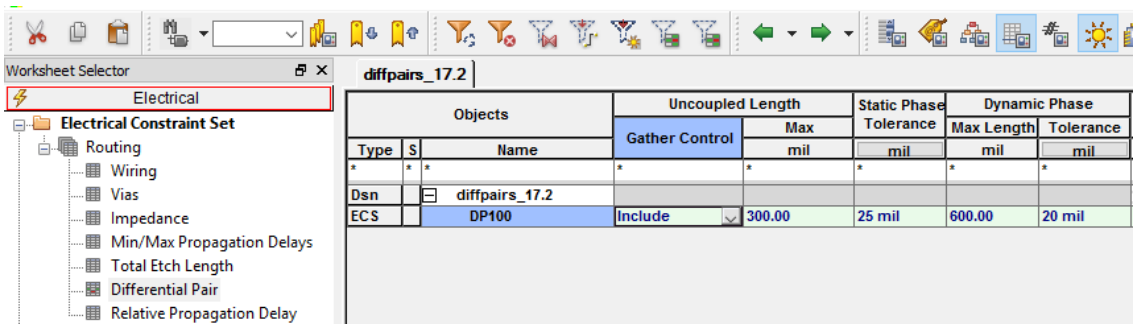
The Dynamic Phase check is designed to meet the guidelines that suggest that the path lengths of the true and complement signals within the differential pair must differ by no more than “x mils” along the entire path of the net. If at any point on the net, the skew between true and complement exceeds “x mils”, this mismatch needs to be compensated within “y mils”. Representative values for x and y might be x = 20 and y = 600.

The constraints associated with Differential Pairs support Static and Dynamic Phase. The margins of each constraint can be set independently using length or time. The Max Length (running skew) constraint for Dynamic Phase is limited to length only.

Static Phase Tolerance – a one-time check from Driver to Receiver comparing lengths or delay of each member. If a Driver cannot be determined, the check is performed across the longest path of the pair.

Dynamic Phase – Etch length of each member is compared at each bend point interval across the Driver-Receiver path of the Diff Pair. Etch length is always measured back to the Driver pins.

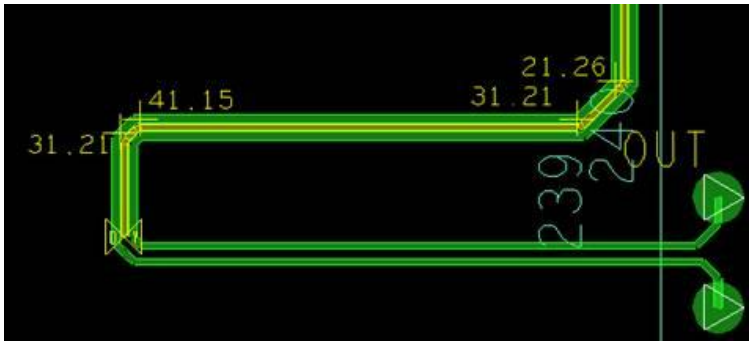
Dynamic Phase Max Length – When specified, the Diff Pair is permitted to exceed the phase tolerance constraint for a contiguous etch length of less than or equal to the value of Max Length specified. If no compensation is made within this specified distance, a DRC will be reported at the point where the Diff Pair first goes out of phase.



As an example, suppose your Dynamic Phase constraints are set as follows:

Static Phase Tolerance	Dynamic Phase	
	Max Length	Tolerance
mil	mil	mil
*	*	*
20 mil	300.00	20 mil

When the DRC is updated, it shows the following:



The beginning of the yellow pseudo line (closest to driver) is where the Diff Pair initially goes out of Phase (beyond the 20 mil Static Phase tolerance). The DRC marker *D-Y* is placed at the initial 'out of phase spec' location as measured from the Driver Pins.

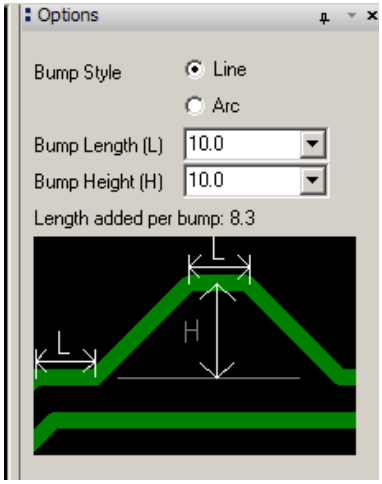
Notes:

- There can only be 1 DRC marker on a pair, even though there may be multiple violation zones.
- It is assumed that the designer will correct the phase issues working from the Drivers to the Receivers.

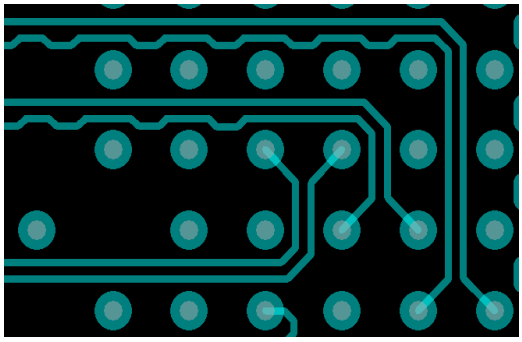
Differential Phase Tuning

Phase Tuning is an alternative to using the mouse guided delay tune command and offers the precision of finite length adjustment to differential signals that are length/phase constrained. It is especially effective on static or dynamic phase-constrained Differential Pairs where iterative etch compensation may be required at various points along the path of either member of the pair. Simply make a mouse click at any point on the cline path to add in a single-parameterized phase bump.

The command is located in the Route Menu of the PCB Editor. When invoked, parameters can be set in the Options panel. Select a style of Line or Arc then define its respective length/size parameters. The form will compute the added compensation for each bump before applying you it.



Phase Tune Options



Differential Phase Bumps