Translating an Existing OrCAD Layout Design to PCB Editor

The object of this article is to provide a worked example of the entire translation process of existing OrCAD Layout design data to OrCAD PCB Editor. The design selected is quite old, actually from the 10.5 installation samples, and deliberately contains many of the relaxed requirements that Layout accepted in the part, netlist and footprint data, since this is likely to more accurately reflect the data that most users would have. In fact this design illustrates many translations issues few of which would be encountered in a more typical design. Before staring any translation, ensure that the design data is synchronised – schematic and PCB data matches.

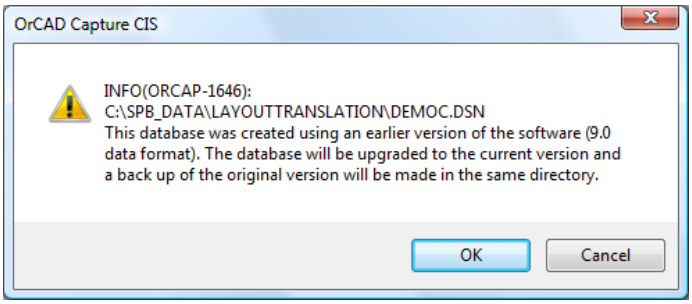
Translation of the board data and the updating of the schematic data

From the 16.2 release the translation process has been incorporated into OrCAD Capture to enable the Schematic footprint property to be updated to match the translated footprint symbol names. The OrCAD PCB Editor flow imposes more restrictions on naming conventions to ensure a greater level of data quality than OrCAD Layout used to require. Whist this means some initial changes to symbol naming, in the longer run data quality and reliability is improved.

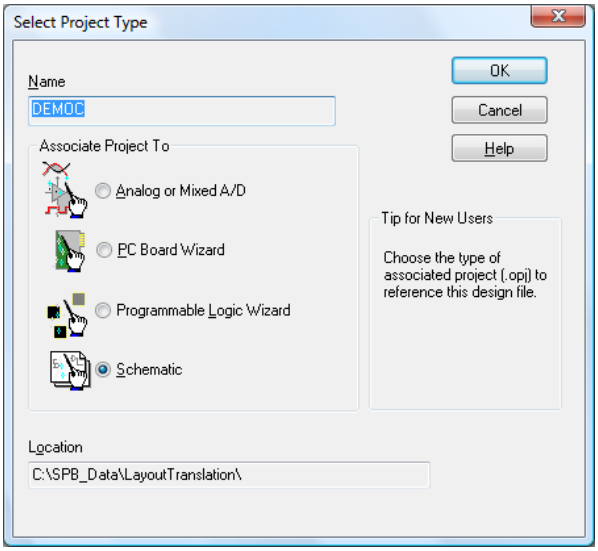
Start by taking a copy of the schematic DSN and board MAX files, it is likely that you will want to ensure that you keep archive copies of the data, and save these to a local directory that you are going to use for the conversion process. In this specific case, the data is going to be in “C:\SPB_Data\LayoutTranslation”.

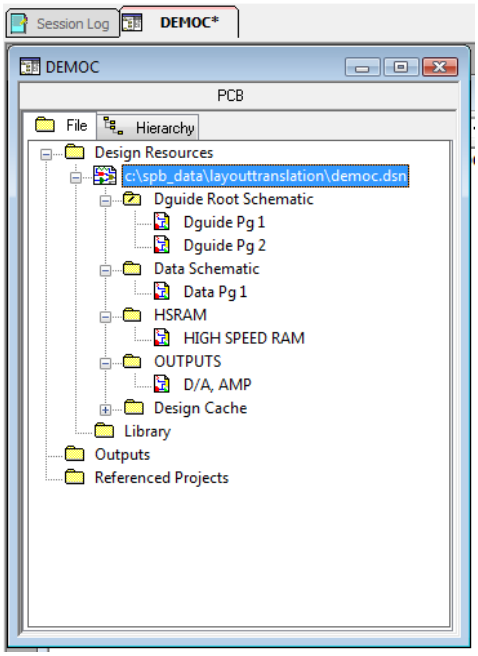
(To follow the process documented in this note, the files being used are in the “tools\Layout\samples\democ” directory within the OrCAD product installation for versions prior to 16.3, the schematic file is demo.dsn and the board file is democ3.max, although not a required change, the MAX file has been renamed to democ.max for this process)

Open OrCAD Capture, or Capture CIS, and then use File>Open>Design, browse to the copy of the saved DSN file, and open the file. Since this design data was created prior to version 16.3, the database format will also be converted to the 16.3 file format.



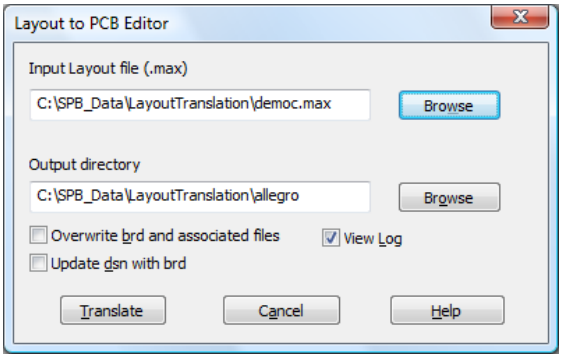
Take OK to convert the project, and then create a project file for a Schematic.





Select the DSN file entry in the Project Window and go to Accessories>Layout to PB Editor Translator>Layout to PCB Editor.

Using the upper Browse button, locate the copy of the MAX file, this should already be in the directory with the DSN file, and select it, the dialog will then be filled in like this:



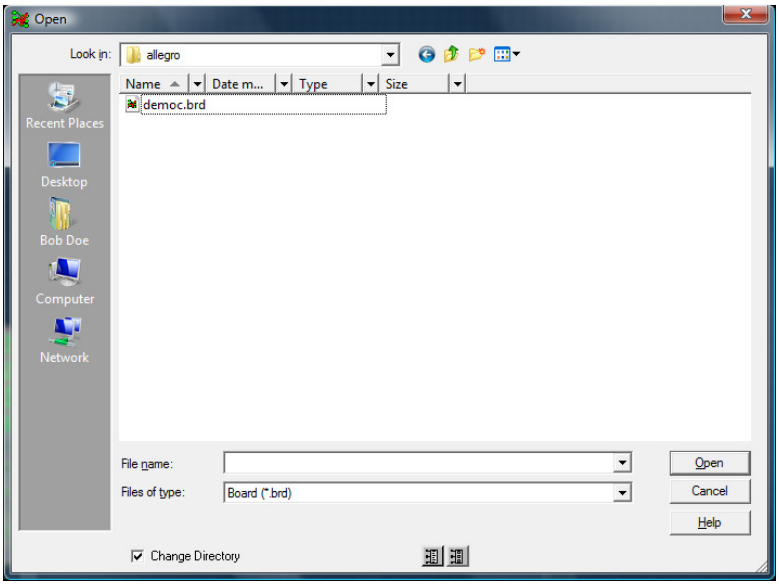
Check the two boxes for “overwrite files” and “update the DSN”, and then left-click on the Translate button to run the translation process. During the processing, you will be prompted to update the footprint data in the DSN file, since a copy of the data is being processed, left-click on OK to make the changes.

When the processing is complete, the changes made to the footprint property in the schematic will be displayed in an “l2a_sync.log” file opened in Notepad. For future reference, this file will be saved in the output directory specified for the translation process.

For the time being, the Schematic data can be saved and OrCAD Capture, or Capture CIS, closed.

Next Processing the Board data

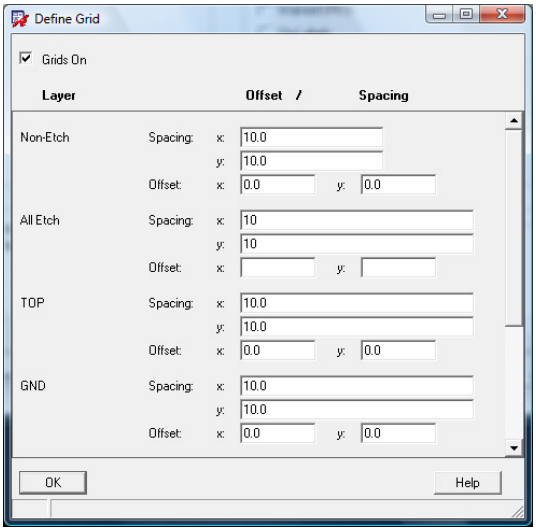
A BRD file called “democ.brd” will have been created in the output directory, in this case, the “allegro” directory under the original Capture DSN file. Start OrCAD PCB Editor and, using File>Open, browse to the democ.brd file, and check the “Change Directory” box on the open file dialog if it is not already checked.



Click OK to the message about being saved with a higher level tool, the board will then be displayed in the PCB Editor canvas.

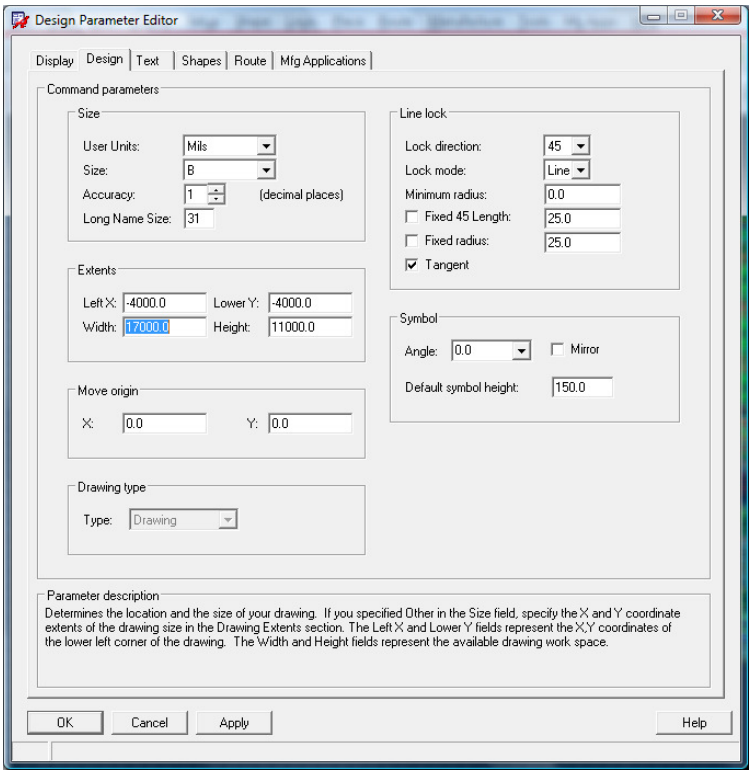
Check that there are no “fixed” properties attached in the design, left-click on the Unfix  toolbar button, move to the background of the design canvas and right-click>Unfix all, then right-click>Done (or F6 on the keyboard).

Now use Setup>Design Parameters to change some settings, these are not essential steps at this point but they will help later in the processing. On the Display tab, set the DRC marker size to 100 (this will make the DRC markers more visible), and left-click on the Apply button to make the setting. In the Grids box, check the Grids On box and use the “...” button next to Setup grids to open the Define grid dialog. Set all the grids to 10, as in the following figure.

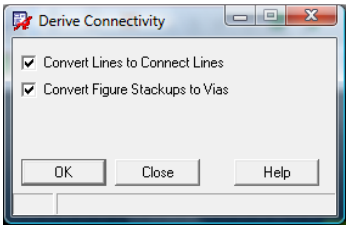


Left-click on OK to accept the changes to the grid settings.

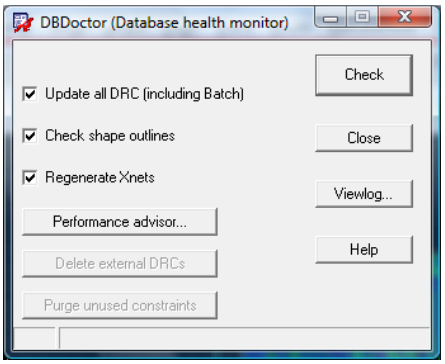
On the Design tab, change the Size to B and both the Left X and Lower Y settings to -4000 and left-click on OK to accept the changes and close the dialog.



Now run some processes to check and correct the data. From the menu select Tools>Derive Connectivity, check the boxes for “Convert lines to connect lines” and “Convert figure stackups to vias” and then left-click on OK to run the process.

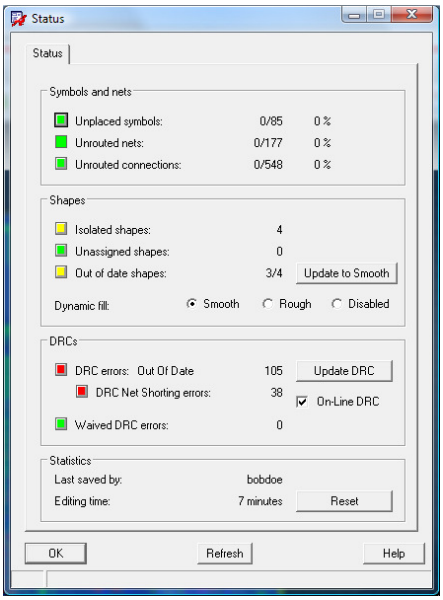


Now, from the menu, select Tools>Database Check, check the boxes for “Update all DRC (including batch)”, “Check shape outlines” and “Regenerate XNets” (just in case), then left-click on “Check” to run the check.



Left-click on “Close” to close the database check dialog.

Having completed the processing, use the Display>Status from the menu to check the current design status.



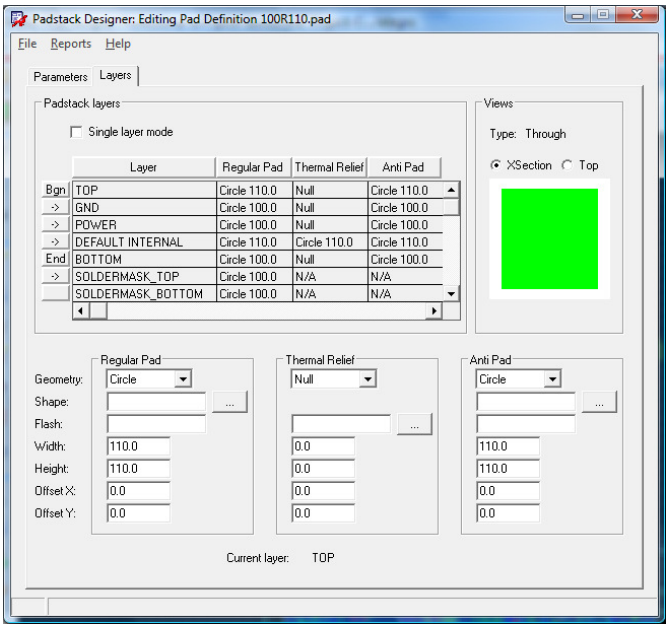
Note that, in this case, there are some DRC errors and one of the shapes is out of date. Left-click on the “Update to Smooth” button to get the shapes re-checked, then left-click on the “Update DRC” button to refresh the DRC status. The Button to the left of the label “DRC errors” will turn to Yellow and the label will change to “DRC errors: Up to Date”. Left-click on the Yellow button to the left of “DRC errors: Up to date” to get a list of the current DRC errors. The majority of the DRC Errors will be “Thru Pin to Thru Pin” and “Thru Via to Thru Via” Spacing errors and will be due to the use of negative planes in the original design. In Layout, the use of negative planes meant that the pad definition used on the plane layer would have included a clearance for the pad. During the conversion these negative planes were changed to positive dynamic shapes and, for positive dynamic shapes, PCB Editor will have added the DRC clearance so, effectively, the required clearance will have been added twice, one to the original pad design in Layout and another for the shape clearance in PCB Editor. In this design the following 12 padstacks need to be edited:

100R110, 110R79, 62R38, 62S38, DIP100T_LIB_PAD3, DIP100T_LIB_PAD4, DIP100T_LIB_PAD5, T1, T2, T3_1, TM_AXIAL_LIB_PAD3, VIA1.

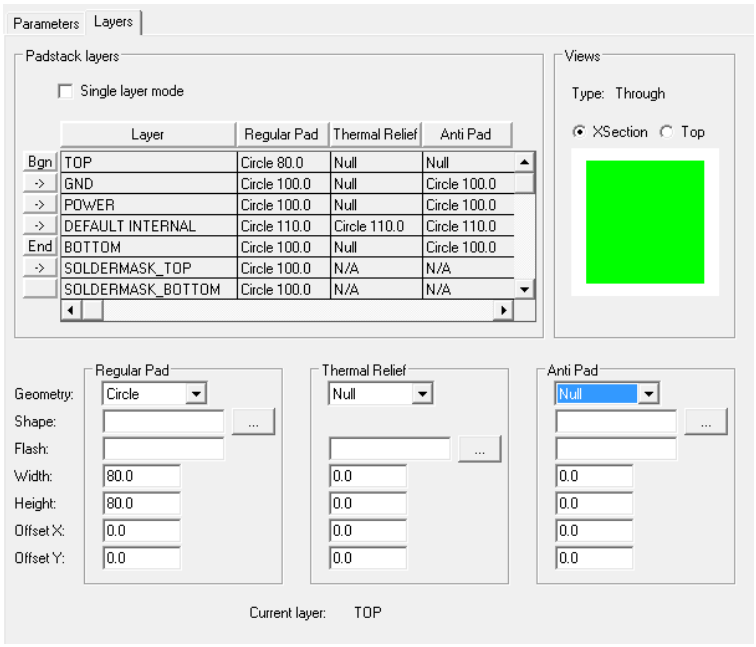
From the menu, use Tools>Padstack>Modify Design Padstack, then, hover over the Options tab and use the "push pin" to fix the tab in the expanded position. The list of Design Padstacks will be displayed in the Options tab.

*Start of the padstack processing:

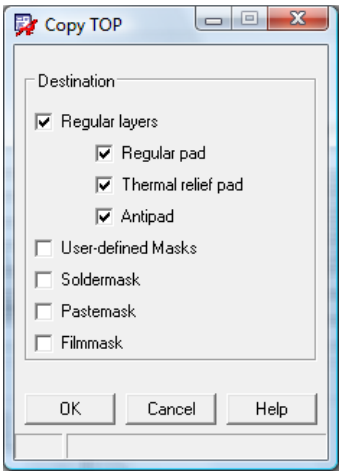
Double-click on each padstack in turn to open the Padstack Designer. When the Padstack Designer opens, left-click on the Layers tab to activate it.



For this specific pad, the drill and the pad are both set 110, then intention being to remove the pad. A better practice would be to set the pad to be smaller than the drill to ensure that there were no small remnants of the pad after drilling, as such, left-click in the TOP (layer) cell, set the Regular Pad to, say, 80 and set the Thermal Relief and Anti-Pad to "null" as shown.



The pad definitions will need to be copied from the Top layer to all the other Etch layers, so right-click on the "Bgn" label and select "Copy to all", this will open the following dialog:



Left-click OK, to perform the copy.

(Note: since positive dynamic shapes are used throughout, there is no need to set the definitions of Thermal Relief and Antipad – these will be taken care of by the Global Dynamic Parameters for shapes in the design)

Use File>Update to Design and Exit to update the padstack in the design, close any warning window that appears and accept the pad update with warnings.

(Note: the 100R110 padstack will also have a warning about the pad being drilled away, this is OK as well)

Repeat the process from "*Start of the Padstack Processing" to this point for the 12 through padstacks listed on page 9. For these, set the Thermal and Anti Pad sizes to "null".

When all of the padstacks have been processed, move the mouse to the PCB Editor canvas and use right-click>Done (or press F6 on the keyboard) to end padstack editing.

The "Pad to Pad" and "Via to Via" DRC markers will have been removed by changing the padstacks and there may be a few errors remaining. In this specific case, there are 7 remaining; three are caused by components overlapping the board outline. These DRC could be waived through Display>Waive DRCs>Waive and left-clicking on the connector DRCs, a prompt for a comment will appear to allow the reason for waiving the DRC to be recorded OR a property attached to the component to allow overlapping of the board outline. To set the property, go to each connector in turn, left-click to select the Package Geometry / Place Bound Top and right-click>Property Edit to open the Property Editor, in the Available Properties list, find and left-click on the "Nodrc_Component_board_overlap" to select the property and left-click on OK to attach the property.

For now the remaining DRCs will be ignored, since they are caused by a small difference in the Etch Line to Line spacing, they will be corrected later.

Set the Artwork format for the shapes; from the menu, Shape>Global Dynamic Params, on the Void Controls tab, set the artwork format to Gerber RS274X in the drop-down and left-click on OK to accept the setting. The shapes in the design will be updated to match the new artwork format.

Now check the remaining DRCs, from the menu, Tools>Quick Reports>Design Rules Check report. In this case there are two locations where the line to line spacing is (just) below the required spacing, since two nets are

involved in each case the DRC is reported twice. In the report window, left-click on one of the “blue links” for the location in the design, the PCB Editor canvas will then centre at that point. (Zooming into the board will probably assist at this point, use either the roll of the mouse wheel, View>Zoom In from the menu, or use the “+” Zoom In Icon) From the menu, pick Route>Slide and left-click on a trace in the canvas that is causing the DRC to begin sliding the trace, once the DRC is cleared, right-click>Done to end the slide mode. Repeat this process for the other DRC location to clear that DRC. Notice that, when the etch segment is selected and the slide started, PCB Editor will attempt to “jump” the segment to a non-DRC position, if that is possible.

(Note: if running on a different design file, there may be different errors reported)

[Optional: From the menu select Display Status. Everything is looking fine now from a connections and DRC standpoint, there are four isolated shapes reported in this example. These are at the centre of the TO99, 8 pin circular parts. If required, these can be removed with Shape>Delete Islands, use the Options tab to select the GND and POWER layers and remove the two isolated shapes from each layer using the “Remove all on layer” button. (In a more typical example there might be many more isolated shapes and the buttons on the Options tab could be used to set through or report on the isolated shapes in the design)]

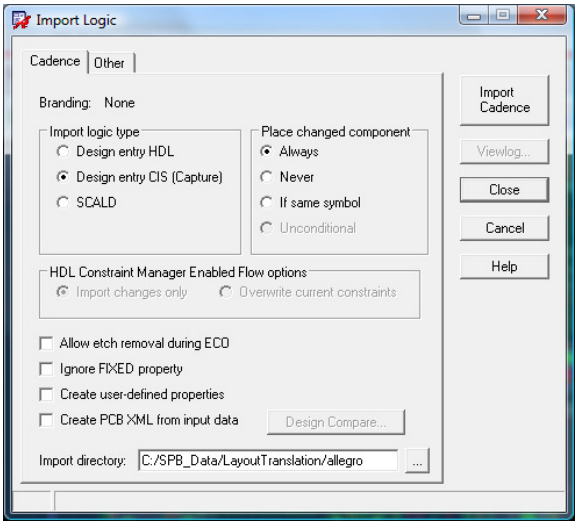
The design is pretty much ready to go now, save the board from PCB Editor and close the application.

Synchronising the Board data

Start OrCAD Capture or CIS and open the “demo” project used for the translation. With the DSN file selected in the Project Window, select Tools>Create Netlist from the menu. Using the sample data the netlist creation will fail because the Inductor component has pin names but no pin numbers, the message states “Pin Number missing from ... All pins should be numbered”. The Pin Numbers will need to be added before the netlist can be created. (Skip this section if the netlist was correctly created with other design data) In the Project Window, open the Dguide Root Schematic and then Dguide Pg2. Get the lower left corner of the schematic in view so that the Inductor L1 is in view. Left-click on L1 and right-click>Edit Part to open the Part Editor, double-click on the Pins in turn to open the Pin Property dialog and set the Pin Number to the same value as the Pin Name in each case. Close the Part Editor and select “Update All” to correct all the inductor parts in the schematic. (Save the design and OK any prompts as the Edit Part session is closed and the schematic is updated). After making any corrections, run Tools>Create Netlist again, this will result in the netlist (*.dat) files being written and attached to the Project.

Start OrCAD PCB Editor, if it not already running, and, if required, open the BRD file from the previous processing. To ensure that there is a backup copy of this data, use File>Save As and specify a board file name of “prenetlist.brd”. So that the Footprint symbols can be checked when the netlist is imported, the existing symbols will need to be exported from the board. Use File>Export>Libraries, use the “...” button to browse and create a “symbols” directory in the board file directory, then use the Export to export the libraries. (This local symbols path will just be used for processing this design)

Then use File>Import Logic to open the Import Logic dialog, set the options as in the following figure:



(Note the directory may vary if using different design data or locations)

Left-click on “Import Cadence” to import the netlist data. Note that using the sample data, the netlist has failed to load due to pins on the footprint not having a matching definition in the schematic symbol. In the case of the specific data used, the footprint assigned to U7 is incorrectly a 24-pin DIP, rather than an 8-pin DIP! This will need to be corrected in the schematic – in fact the “Instances” Footprint property for this part is correct.

For the other parts, since these pins are not connected the “NC” property and a comma separated list of pin numbers can be attached to the parts. For the sample data, go to the schematic and use Edit>Properties to add the NC property and values as shown in the following table:

J1	65,66
J2	3,4
J3	3,4
U3,U4,U8,U9,U10,U11,U12,U13	1,8,9,16,17,24,25
U16	5,26,27,38,47,55,59,68
U18	5,6,7,8
U22,U23	1,5,8

(Double-click on the part to edit the properties and use New Row, or New Column, to add a new property, set the name to NC and the value to the list of pins reported above.)

When all the NC properties have been added, close the Edit Properties dialog, save the design and create another netlist with Tools>Create Netlist.

In the PCB Editor Command Window, type reopen and <enter> this will reload the “prenetlist” board, if prompted, don’t save the data. Then use File>Import>Logic and setup the import as before. Now, when the import processing is completed, things are looking a lot better and components have not been removed from the board.

Remaining issues - Mounting holes, not in the netlist

The final issue with the sample data is the mounting holes. In Layout, these components were added directly to the design and were not part of the netlist, and equally therefore, won’t be part of the PCB Editor netlist. The parts were added to the design during the original process because they have reference designators and pin numbers. PCB Editor handles “not in netlist” parts differently using specific “mechanical symbols”, these have

none, or more, mechanical pins and are not connected to nets in the design. To complete this part of the process a new mechanical symbol will be designed based on the existing symbol that was translated.

PCB Editor is used to create and modify symbols so use File>Open to start the editing process, if prompted to save the existing board, DO NOT save this over the “prenetlist” board use another name, like “finished1”, the “prenetlist board will be needed! With the Open File dialog running, change the “Files of Type” drop down to “Symbol Drawing (*.dra)”, browse into the “symbols” directory created when the Libraries were exported earlier, find the “mthole1.dra” and open the file.

Use Display, Color / Visibility, pick the “Components” entry on the left, pick a colour other than black (the background colour) by left-clicking on a colour “chip” in the “Color” group and then apply it to all the Ref Des entries by left-clicking in the “All” cell under Ref Des, left-click on OK to close and apply the colour change. None of the text is required for a mechanical part so use Edit>Delete from the menu, on the Find Filter use the “All off” button and then check “Text” to have text as the only active type, drag a box around all the items on the canvas and use right-click>Done to accept the change. Then go to Setup>Design Parameters, select the Design tab, and change the Drawing Type drop-down to Mechanical, then OK to make the change. Save the new symbol using File>Save, set the file name to “mthole”, note that the DRA file is saved and a BSM file is also created.

Open the “prenetlist” board again, either use File>Recent Designs, or File>Open (remember to change the “Files of type” to *.brd if using File>Open). There are 3 mounting holes to replace in the sample design. Use Place>Manually to get the placement function started. On the Advanced Settings tab, check the box for “Library”. (The required mechanical symbol is not currently in the database so this setting will allow “any” available symbol to be placed). Also check the “Autohide” button, this will hide the placement dialog while the component is being placed. Change back to the Placement list tab and pick Mechanical Symbols from the drop-down at the upper left of the dialog. The available mechanical symbols will then be displayed in the list. Check the box to the left of the MTHOLE entry and move the mouse into the canvas, repeat this until 3 of the MTHOLE parts are placed on the canvas, the exact position is not too important as long as they are outside the board outline. Use OK to close the placement dialog when finished.

Now the components just added are going to be moved to the required locations for the mounting holes. The existing components could be deleted and the new ones moved to the required locations but it is easier to swap the component placements and then delete the “old” components from the outside of the board. From the menu, pick Place>Swap>Components, left-click on the new mounting hole and then left-click on the existing one, the components will be swapped, repeat this for the three mounting holes and right-click>Done when completed. Now the “old” components need to be deleted, use Edit>Delete from the menu, on the Find Filter, use “All Off” and set Symbols to restrict what is deleted and then select the “old” mounting hole components. (If they are in a group off the board, the easiest way to select them is by dragging a box around them, otherwise, use left-click on the first one and control+left-click on the others to make a group) When selected, use right-click>Done to accept the change. Now that the mounting holes have been changed, the netlist can be reloaded using the previous process.