Introduction

Microvias as defined by the IPC are vias whose diameter is less than 6 mils with capture pads less than 16 mils. There are several processes that can be used to form the Microvia such as Plasma, Photo Imaging, Wet Dry Etching however the most popular used today is Laser ablation. IPC projects Microvia usage to increase as package pitch decreases. While .5 or even .4 mm pitch packages are used today especially in the wireless/consumer electronic industry sector, plans are underway for package pitch pushing .30 and .25 mm.

Microvias are commonly used in stack-ups similar to the one shown in figure 1 courtesy of IPC 2226. This stack-up is probably the most commonly used stack-up used in the industry for HDI Design. Cost efficiency is achieved by limiting both the number of laminations and use of stacked vias. As package pitch continues to decrease, the used of stacked Microvias or stacked Micro to Core vias may become more common.

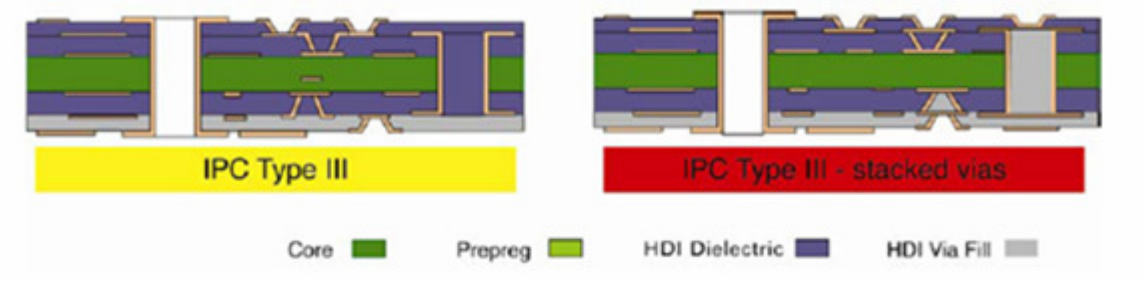
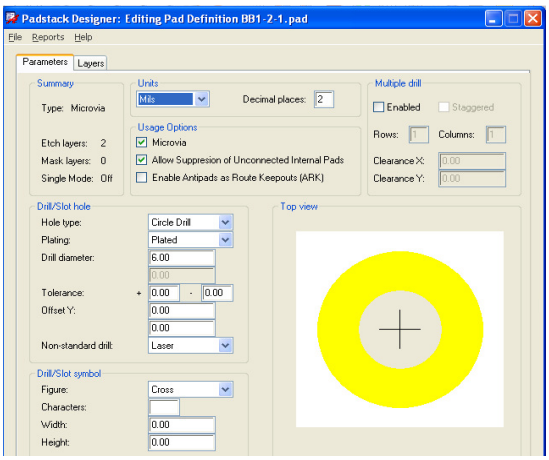


Figure 1 – HDI Type III Stack-up

While Allegro currently supports B/B Vias, the newly established Microvia is necessary to setup the clearance matrix associated with the technology. This includes but not limited to “Microvia to Microvia” and “Microvia to Core Via” spacing rules. Prior to 16.2, all non-standard vias (buried and blind) were categorized by the database object “BB Via”. In addition, the Same Net DRC system was not robust enough to differentiate net to net from same net spacing rules; specifically the Same Net system derives its values from the Net to Net rules.

Microvia Padstack

The Padstack Editor now supports a “Microvia” Usage option. This option is limited to B/B via types and is primarily used to drive HDI spacing rules between it and other metal objects in both the Spacing and the new Same Net Spacing domains in Constraint Manager.



Usage Options

3 usage options can be associated with the padstack.

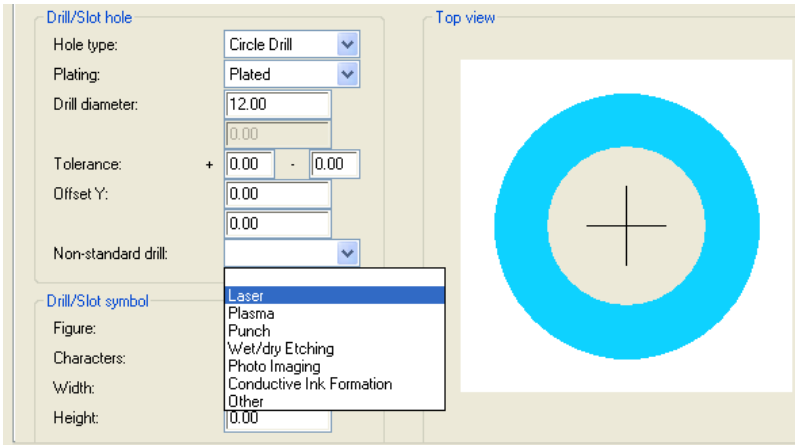
- **Microvia** – Use on HDI boards where spacing rule sets differ between HDI and convention B/B or Core vias. The Microvia usage option can only be applied to a B/B via type. The B/B via type should be used to represent mechanical drilled vias such as the Core via on an HDI design. The 2 via types are supported in the Spacing and Same Net Spacing Constraint Domains of Constraint Manager.
- **Allow Suppression of Unconnected Internal Pads** – Enable to allow unused inner layer pads to be suppressed as a function of artwork generation or with the new database driven Unused Pad Suppression application introduced in 16.2. This usage option replaces the former Internal Types of Fixed or Optional; basic functionality remains the same.
- **Enable Antipads as Route Keepouts (ARK)** – Enable to use antipads associated with Mechanical Pins as an implicit route keepout area. This may reduce the need to draw keepout shapes associated with the Mechanical Symbol. Use in combination with the Design Level Mechanical Hole DRC checks.

Non Standard Drill Types

Non-standard drill types are attributes associated with the padstack that are used exclusively by the NC Drill programs for the purpose of sorting NC files. These attributes do not factor in any DRC checking.

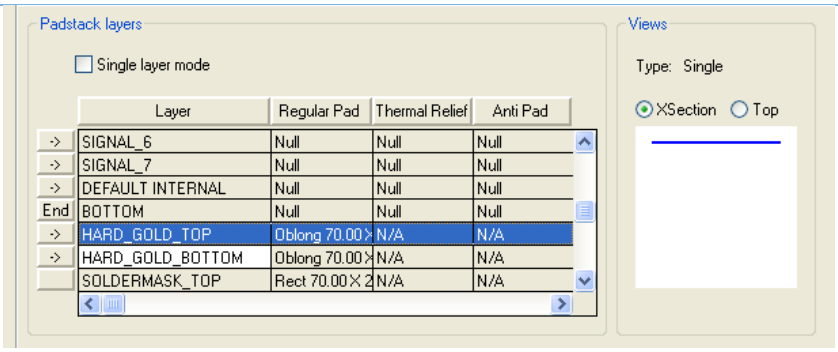
3 additional HDI related drill types were added in the 16.2 release.

- Wet/Dry etching
- Photo Imaging
- Conductive Ink Formation



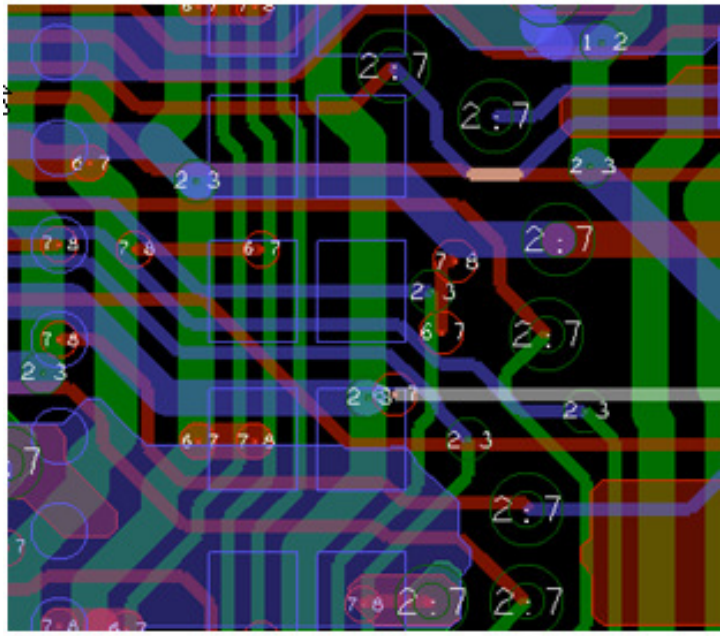
User Definable Mask Layers

The Padstack supports up to16 user-definable mask layers. Mask layers can be used for custom applications such as via plugging, filling, gold deposition to name a few. DRCs are not performed on these layers.



B/B Via Span Labels

Via span labels serve as a graphical aid in identifying the begin/end layers of a B/B via. Numeric's within the extents of the pad indicate the begin/end layer of a single via or a series of stacked vias. A colon between the begin/end layers indicates the span of a single B/B via; a dash represents a stacked series of B/B vias. The display is based on a global control. The default color of the label is white but is customizable through the color dialog. Layer numbers are ordered in an ascending numerical sequence, e.g. Layer Top = 1, Inner Layer 1 = 2, Plane 1 = 3 and so on. The mapping between the display and actual layer names is not user configurable. Labels do not appear on through-hole vias or pins.



Via List Enhancements

The Via List, a member of the Physical Constraint Set, has been enhanced to support bitmaps and Start/End layer fields to help identify the type of via and its range. The list represents a selectable order of vias when used with the Add Connect command. For example, the graphic below suggests BB1-2 be the priority via when transitioning from Layer Top to Signal_2; the alternative being the thru-hole via VIA019.

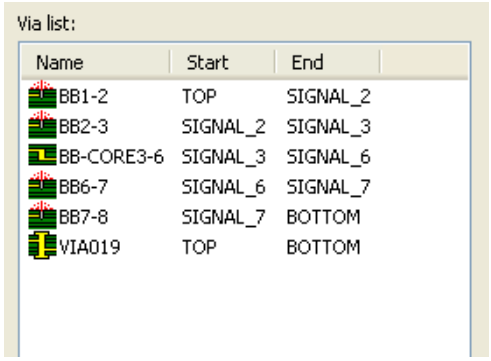
Blind or Buried Via

Through Hole Via

Microvia

Die Pad

Surface Mount Pad



Foundation for HDI Rules

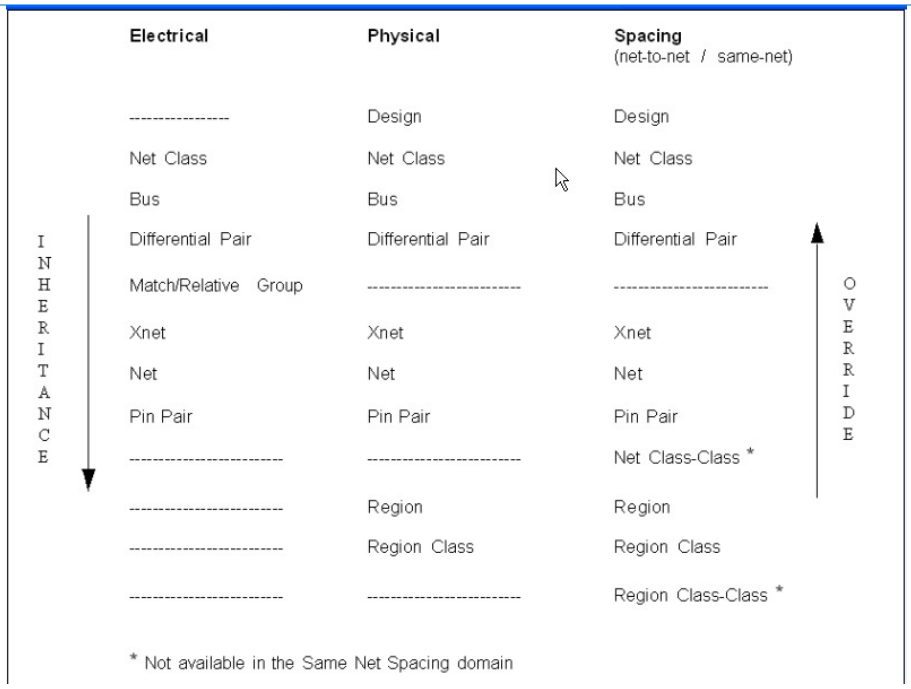
The Same Net DRC system drives the rules for via staggering and overlap (Inset) used on HDI Designs. From SPB16.2 this provides the spacing differentiation for the following via combinations:

- Microvia to Microvia
- Microvia to Core Via (represented as B/B Via)
- Microvia to Thru-hole
- Core Via to Core Via
- Core Via to Thru-hole

The Same Net DRC system supports rules for via tangency (vias that touch) and inset (vias that overlap). Stacking will continue to be controlled by settings in the Physical Domain. Etch Edit applications have been enhanced to align with the changes made to the Same Net DRC system. A new add-via model adds via structures while obeying same net rules. The bubble code is aligned with the same net rules making the sliding of vias to other vias or pins on the same net more efficient. Stacked vias are seen as a group entity with controls for breaking the stack when necessary.

Constraint Manager – Same Net Spacing Domain

Same Net Spacing rules released in 16.2 are now managed entirely within the new Same Net Spacing Domain in Constraint Manager. Each Spacing DRC is represented by an equivalent Same Net DRC. The Same Net Domain is structured similar to the Spacing domain following the rules established for constraint inheritance and overrides. Constraint Objects not supported in the domain are Net Class-Class and Region Class-Class since they are used exclusively for net-net rules. The table below indicates the hierarchy used to manage the Electrical, Physical and Spacing rules.



	Electrical	Physical	Spacing (net-to-net / same-net)
INHERITANCE ↓	----------	Design	Design
	Net Class	Net Class	Net Class
	Bus	Bus	Bus
	Differential Pair	Differential Pair	Differential Pair
	Match/Relative Group	----------	----------
	Xnet	Xnet	Xnet
	Net	Net	Net
	Pin Pair	Pin Pair	Pin Pair
	----------	----------	Net Class-Class *
	----------	Region	Region
	----------	Region Class	Region Class
	----------	----------	Region Class-Class *

* Not available in the Same Net Spacing domain

↑ OVERRIDE

Via-in-Pad Overview

Via-in-Pad is a common fanout strategy used on HDI designs, especially on BGAs with package pitch of .8 mm or less. With Via-in-Pad, component placement can be more compact; capacitors can be placed closer to the device pins they need to bypass. Via-in-pad also has its drawbacks as it can introduce soldering issues in manufacturing. Solder can wick down through the open holes, if not plugged, drawing solder off the component pad.

Different rules may exist for metal and soldermask defined pads. For metal defined pads, a via should be contained within the bounds of the SMD pad otherwise the solderpaste will spread out to include the via resulting in possible tomb-stoning of components.

With soldermask defined pads, a via may be allowed to float within the SMD pad up to the point where the center of the via hole intersects the edge of the SMD pad.

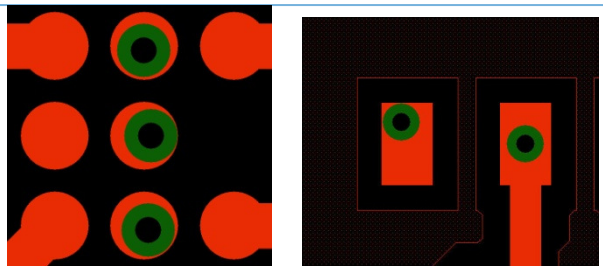
Typically thru-hole vias are not allowed in SMD pads. Thru-hole vias can result in solderpaste flowing down the barrel of the hole. However, capabilities must be there to allow such conditions for thermal, RF shielding and power applications.

Via-in-Pad DRC Suite

A new suite of DRC checks ensures the placement of vias is properly contained within SMD pads. These checks originated in the PCB Router (Specctra) and are now fully integrated into the Allegro PCB Editor. Via-in-Pad checks are run at the design level but override capability at the symbol level is possible with properties.

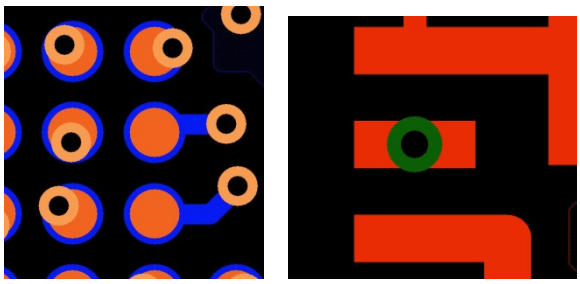
Via at SMD – Fit On

This check is designed for metal defined pad applications where vias must be totally contained within the boundary of the SMD pad. A DRC is generated if the via pad protrudes outside the SMD pad. The examples below show legal via-in-pad placement for this check condition.



Via at SMD – Fit Off

This check is designed for soldermask defined pads where a via is allowed to float outside the edge of an SMD pad up to the point where the center of the via is still inside the SMD pad. Floating the center of a via beyond the edge of the pad would result in acid trap formations. Other applications for this check might include vias placed in narrow SMD pads, ones typically associated with QFP devices.



Via at SMD Thru

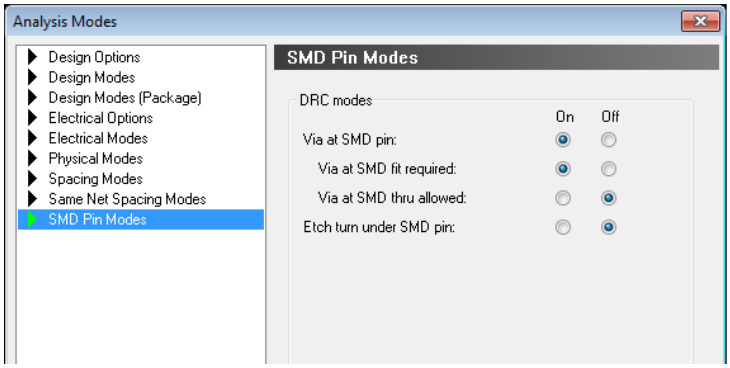
This check is designed to detect placement of thru-hole vias within the SMD pad boundary.

Mode Settings

Mode settings for Via-in-Pad constraints are located in **Constraint Manager – Analyze – Analysis Modes – SMD Pin Modes**. The constraints align with the names used in the PCB Router.

Via at SMD Pin – '**On**' activates the Via-in-Pad DRC Check

- **Via at SMD fit** – '**On'** state = via pad must be contained within SMD pad
- **Via at SMD fit** – '**Off'** state = center of via cannot extend beyond edge of pad
- **Via at SMD thru** – '**On'** state = Thru vias allowed in SMD pads
- **Via at SMD thru** – '**Off'** state = Thru vias not allowed in SMD pads



Property Overrides

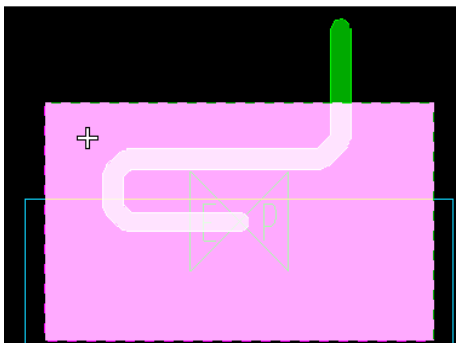
Not all packages may conform to a design level check. It may be common to use Via at SMD Pin 'Fit on' as a Design level check but certain packages may lend themselves to 'Fit Off' behaviour. Specific properties are available for the Via at SMD Pin checks that override the behaviour of the design level check. They include:

Property	Values	Apply to
Via_at_SMD_Fit	On or Off	Pin, Symbol
Via_at_SMD_ Thru	True or False	Pin, Symbol

Etch Turn Under SMD Pin DRC

This check is designed to detect etch compensation buried within the pad. Driven by concern that etch segments within pad boundaries adversely affect timing rules, the checker reports if more than 2 vertex point in located within the pad boundary and by default applies to nets that have timing or length rules. A drawing level property is available to run on all nets if necessary. An exception property exists and can be applied to irrelevant nets.

Property	Values	Apply to
Etch_Turn_Under_All_Pads	True or Off	Drawing
Etch_Turn_Under_Pad_Exempt	True or Off	Net



Add Via Overview

Interactive routing in Allegro is built on the model of active and alternate layer pairs. Its efficiency is limited to 2 layer routing strategies. Changing the alternate layer during routing requires mouse travel to the options panel where a new destination layer and/or via selection is made. Function keys can be mapped to the altsubclass commands in lieu of the mouse travel to the options panel.

A new model based on the concept of multiple alternate layers was introduced in 16.2. The 'Working Layer' model, in combination with a new Via Popup GUI, localizes the steps of layer transition near the point of occurrence. Upon a LMB double-click in the canvas, a GUI appears displaying a list of layers enabled in the 'Working Layers' dialog. A single click on any one of the layers closes the form and adds the vias as determined by the ordering in the Physical CSet.

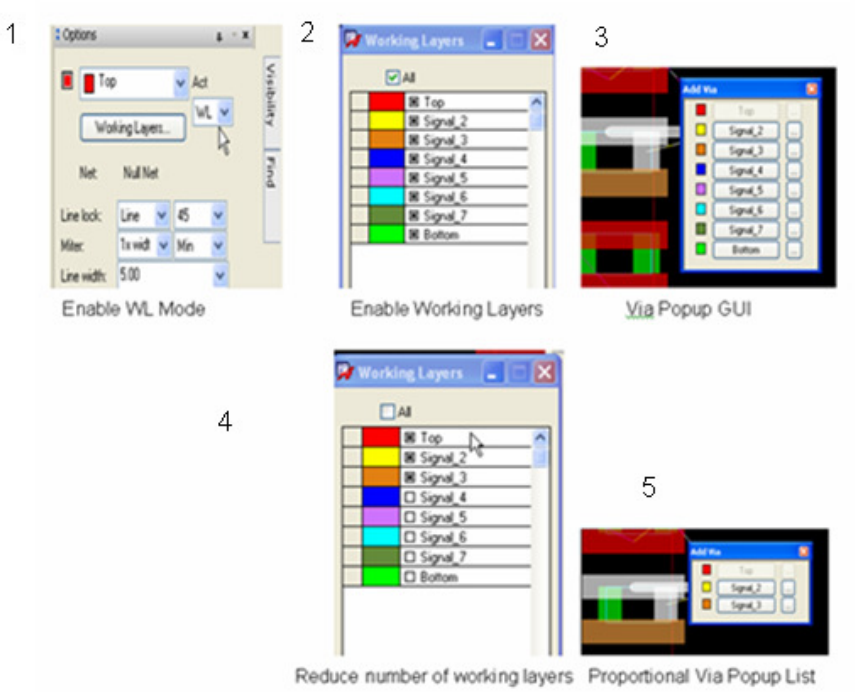
On advanced technology boards such as Type III HDI or ones utilizing Any Layer vias, the new add via model automatically adds a coincident series of stacked vias in just one mouse click or through semi-automatic means, a staggered sequence of vias placed at the minimum same net clearance rules for the respective via types of the structure.

Working Layer Model

The new 'Working Layer' concept is an alternative, not replacement for the legacy active/alternative editing model. While in the Add Connect command, the selection of the dropdown choice 'WL' enables the environment. From there, a Working Layers dialog controls the layers that appear in the Via Popup GUI. The enablement of all layers in the dialog results in a full size Via Popup GUI. On high layer count boards, the list may become too long to efficiently work with, hence enabling a subset of layers, ones known to be probable candidates for layer transitions, is recommended.

The following example outlines the flow for using the 'Working Layer' mode:

1. While in Add Connect command, select WL from pull-down in the Options Panel.
2. Click 'Working Layer' button then enable all layers; close form.
3. When in Add Connect, a double click with the LMB produces the fully populated Via Popup GUI with the Active layer dimmed. Selecting a layer in the GUI adds the via and closes form.
4. 'Working Layer' dialog opened, 5 layers are disabled.
5. A double click during Add Connect produces a shortened GUI with 2 layers available to via to.

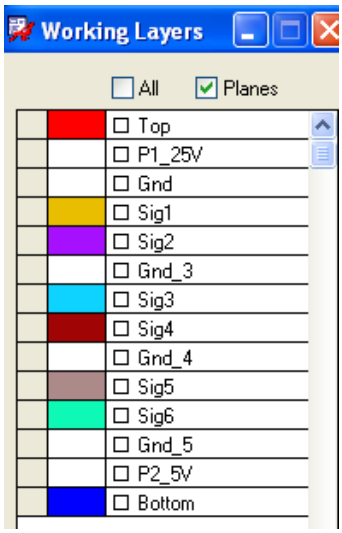


Working Layer Dialog

With the Add Connect command active, access the Working Layer dialog from the:

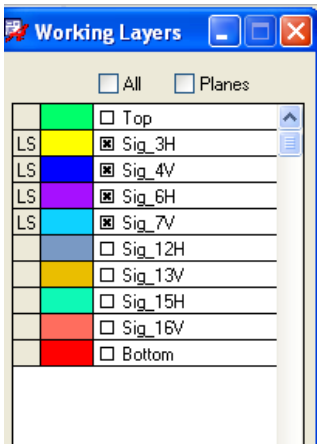
- Options Panel (right side of canvas)
- RMB – Working Layers menu selection

The color swatches that appear in the form align with the colours used for the ETCH subclasses. Plane layer display is an available option when enabled appends all layers classified as PLANE to the list. By default, Plane layer display disabled since it's uncommon to route on them.



Layer Set Identification

It is not necessary to keep the Working Layer form open during routing however the following behavior should be noted when routing nets constrained by Layer Set rules. The first column of the dialog is reserved for LS (Layer Set) identification. Similar to the bolding of layers in the legacy add via model, LS appears adjacent to all layers of the Layer Set definition. These layers will become temporarily enabled if in a disabled state.

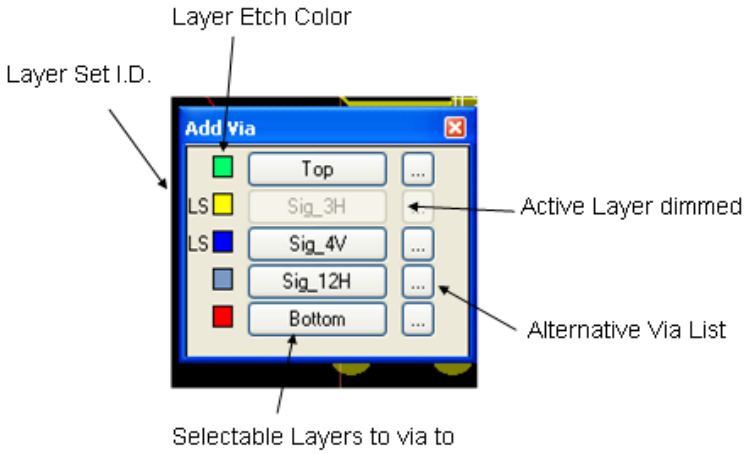


Via Popup GUI

When the 'Working Layer' Mode is enabled, a LMB double-click produces a Via Popup GUI at about the location of the via to be inserted. The layers that populate the GUI are driven from the 'Working Layer' setup form with the Active layer always dimmed out. When only 2 layers are enabled, a LMB double-click adds the via without GUI intervention. This emulates the legacy Active/Alternate model.

The via(s) inserted are driven by the ordering in the respective Physical CSets. This discussed more in the next section. The ellipse buttons on the right side of the form provide access to alternate or least preferred vias based on the ordering within the CSet.

One of the major benefits of the new model is the ability to automatically add sequential B/B vias on the path to the destination layer. If stacking rules are permitted, each via of the stack is added at a coincident location. If stacking is not permitted and staggering rules prevail, each via of the sequence is floated on your cursor spiralling around the previously instantiated via at 22.5 degree increments with respect to the same net spacing rule between the 2 via types.



Ordered Via List

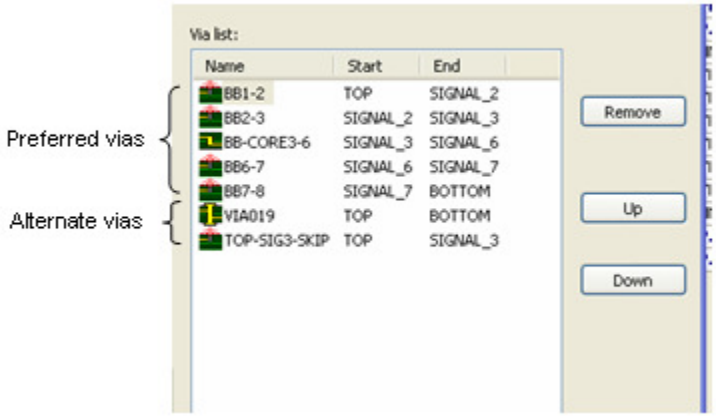
It's common to have preferred and alternative vias associated with many nets that comprise the design. Prior to 16.2, the vias associated with the path from Active to Alternate layer populate the via list but with no special consideration for what is most used (preferred) or least used (alternative).

An example application utilizing an alternate via is with HDI where the priority for most signal transitions through the layers is with Micro and Core vias however a thru-via is present in the via list for special circumstances.

The concept of an ordered via list is to provide a default condition, one that is predictable, when adding a single or sequence of vias through the board. The Via List represents the selectable order of vias used by the add connect command. The order of the vias allows an application to automatically select the first via, or sequence of vias, in the list that meets the desired layer-span. The following guidelines are suggested when working with Via Lists:

- When Microvias and/or B/B-vias are preferred over thru-vias, they should be listed first in the Via List.

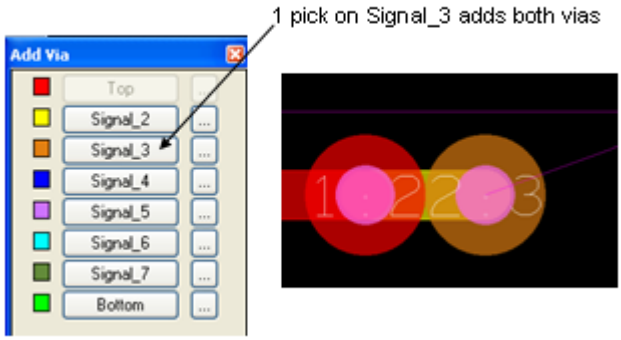
- Each CSet should contain a complete Via List. Vias are not inherited across CSets.
- Any via listed after a thru-hole will not be preferred, since if the thru-hole appears first, it can achieve any start/stop combination.
- Vias are often listed in the order of the cross-section, but this is not mandatory.
- A via will not have priority if its layer-span is achieved by one or more vias listed earlier in the Via List. As an example (BB1-2, BB2-3, BBSkip1-3) BBSkip1-3 is not preferred as the path from Layer 1-3 is achieved by the first two vias in the list)
- Vias that are not preferred can still be added from the Via Popup GUI, though it requires extra mouse picks.
- The drill direction (Up or Down through the cross-section) does not matter. The vias chosen from the Via List will be the same.
- Where different Regions require different Via Lists, it is recommended to create new and customized CSets as required. The Region object supports its own Via List.



Example

Using the Via List in the above graphic, a signal is being routed on Layer Top.

- A LMB double click produces the Via Pop GUI shown below.
- Signal_3 is selected from the list, form closes.
- BB1-2 is inserted at pick point; BB2-3 via spirals around BB1-2 @ 22.5 degree increments.



Using the same example, instead of selecting Signal_3, the ellipse button adjacent to it is selected producing the list of alternate vias to choose from. Selection of either via from the list closes the form and adds the via.

Adding HDI Vias

The new add via model is designed to increase the efficiency of adding HDI vias of the following structure types:

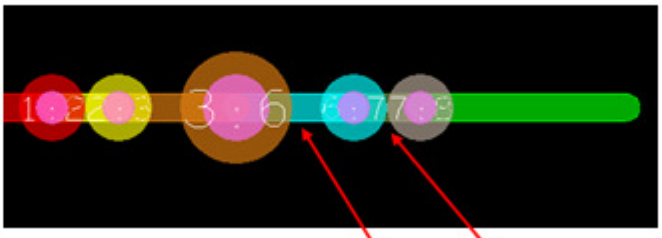
- Staggered
- Stacked Microvias/Offset Core Via
- Stacked Microvia & Core Via
- Inset Vias (Overlapping of vias)
- Any Layer Via

The add via model is based on the selection of the destination layer in combination with the appropriate Physical CSet driven ordered Via List. In the 4 examples below, a transition is made from Layer Top to Bottom.

Example 1 – Adding Staggered Vias

The following vias are used in the sequence (BB1-2, BB2-3, BB3-6, BB6-7, BB7-8). All but BB3-6 are classified as Microvias.

- While routing on Layer Top (1), a LMB double-click produces the Via Popup GUI where Layer Bottom (8) is selected.
- BB1-2 via is inserted at the pick location; BB2-3 is floating on the cursor.
- Remaining vias are semi-automatically added where user has control of location about the previously inserted via.
- Rotation angle about previously inserted via is 22.5 degrees.
- Use CNTL key to go into free angle mode if desired.
- Separation of vias is controlled by the Same Net rules for Microvia to Microvia (0 mils) and Microvia to BB Via (5 mils).



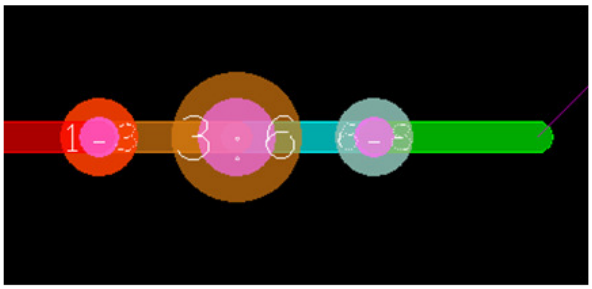
module4_addvia

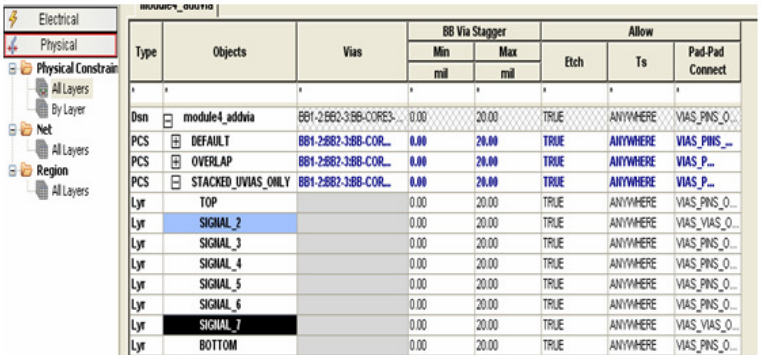
Type	Objects		Microvia To								
		Bond Finger	Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Microvia	Shape
		mil	mil	mil	mil	mil	mil	mil	mil	mil	mil
*	*	*	*	*	*	*	*	*	*	*	*
Dsn	module4_addvia	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	0.00	5.00
SNSC	DEFAULT	**5.00**	**5.00**	**5.00**	**5.00**	**5.00**	**5.00**	**5.00**	**5.00**	**0.00**	**5.00**
Lyr	TOP	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	0.00	5.00
Lyr	SIGNAL_2	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	0.00	5.00
Lyr	SIGNAL_3	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	0.00	5.00
Lyr	SIGNAL_4	5.00	5.00	5.00	5.00	5.00	5.00	5.00	5.00	0.00	5.00

Example 2 – Adding Stacked Microvias

Similar to Example 1, the following vias are used in sequence (BB1-2, BB2-3, BB3-6, BB6-7, BB7-8) however in this example, rules permit the stacking of BB1-2 to BB2-3 and BB6-7 to BB7-8. The Core via (BB3-6) is offset from the stacked vias.

- While routing on Layer Top (1), a LMB double-click produces the Via Popup GUI where Layer Bottom (8) is selected.
- Both BB1-2 and BB2-3 vias are inserted coincidently (at same x,y location) at the pick location; BB3-6 via is now floating on cursor.
- Physical CSet rules to allow stacking include:
  - Min BB Stagger set to 0
  - Allow Pad to Pad Connect set to Vias_Vias_only on Layers Signal_2 and Signal_7.
- Label associated with stack provides guidance that more than 1 set of B/B vias are stacked (label 1-3).
- BB3-6 separation from the stacked Microvias is controlled by the Same Net Microvia to BB Via rule of 5 mils.
- 1 LMB pick inserts BB3-6 via; BB 6-7 and BB7-8 (stacked formation) floating on cursor, separation to BB3-6 controlled by Same Net Microvia to BB Via rule of 5 mils.
- 1 LMB pick inserts both BB6-7 and BB7-8 at the pick location.
- The slide command treats the stacked vias as a single entity. Use the RMB – Split Stack command to slide a specific via of the stack.



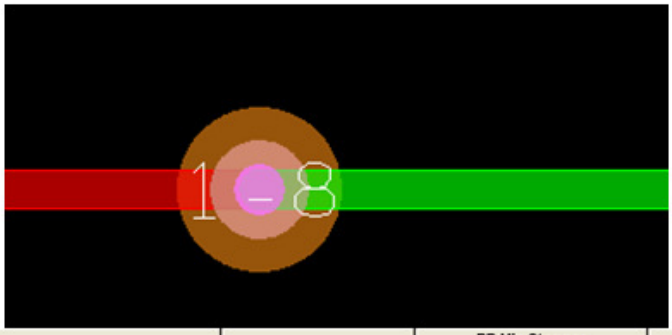


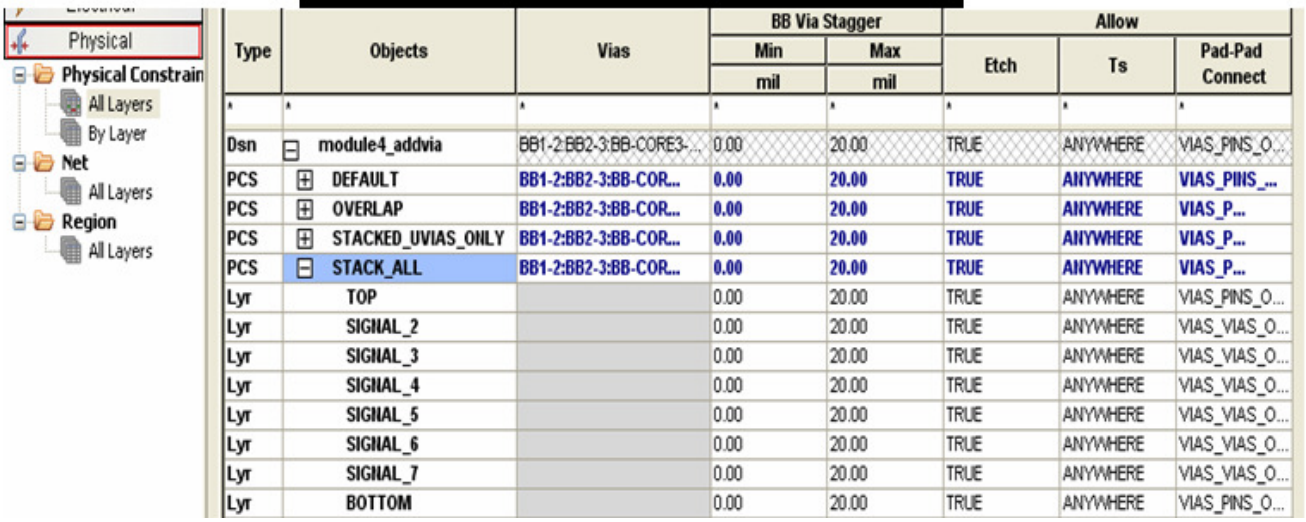
Type	Objects	Vias	BB Via Stagger Min mil	BB Via Stagger Max mil	Allow Etch	Allow Ts	Allow Pad-Pad Connect
Dsn	module4_addvia	BB1-2:BB2-3:BB-CORE3-...	0.00	20.00	TRUE	ANYWHERE	VIAS_PINS_O...
PCS	DEFAULT	BB1-2:BB2-3:BB-COR...	0.00	20.00	TRUE	ANYWHERE	VIAS_PINS_...
PCS	OVERLAP	BB1-2:BB2-3:BB-COR...	0.00	20.00	TRUE	ANYWHERE	VIAS_P...
PCS	STACKED_UVIAS_ONLY	BB1-2:BB2-3:BB-COR...	0.00	20.00	TRUE	ANYWHERE	VIAS_P...
Lyr	TOP		0.00	20.00	TRUE	ANYWHERE	VIAS_PINS_O...
Lyr	SIGNAL_2		0.00	20.00	TRUE	ANYWHERE	VIAS_VIAS_O...
Lyr	SIGNAL_3		0.00	20.00	TRUE	ANYWHERE	VIAS_PINS_O...
Lyr	SIGNAL_4		0.00	20.00	TRUE	ANYWHERE	VIAS_PINS_O...
Lyr	SIGNAL_5		0.00	20.00	TRUE	ANYWHERE	VIAS_PINS_O...
Lyr	SIGNAL_6		0.00	20.00	TRUE	ANYWHERE	VIAS_PINS_O...
Lyr	SIGNAL_7		0.00	20.00	TRUE	ANYWHERE	VIAS_VIAS_O...
Lyr	BOTTOM		0.00	20.00	TRUE	ANYWHERE	VIAS_PINS_O...

Example 3 – Adding Stacked Micro/Core Vias

The following vias are used in sequence (BB1-2, BB2-3, BB3-6, BB6-7, BB7-8) however in this example, rules permit the stacking of all via types.

- While routing on Layer Top (1), a LMB double-click produces the Via Popup GUI where Layer Bottom (8) is selected.
- The entire set of vias are inserted at the pick point.
- The via label is indicative of the complete stacked series of vias (1-8)
- Physical CSet rules to allow stacking include:
  - Min BB Stagger set to 0
  - Allow Pad to Pad Connect set to Vias_Vias_only on all layers except Top and Bottom where settings support Via-in-Pad.
- The slide command treats the stacked vias as a single entity. Use the RMB – Split Stack command to slide a specific via of the stack.



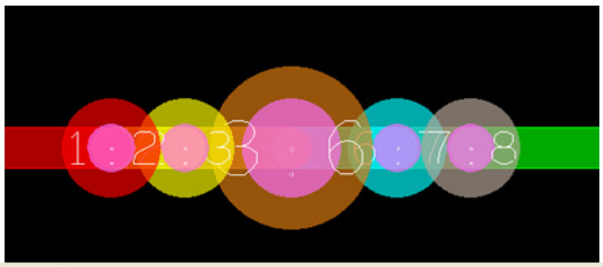


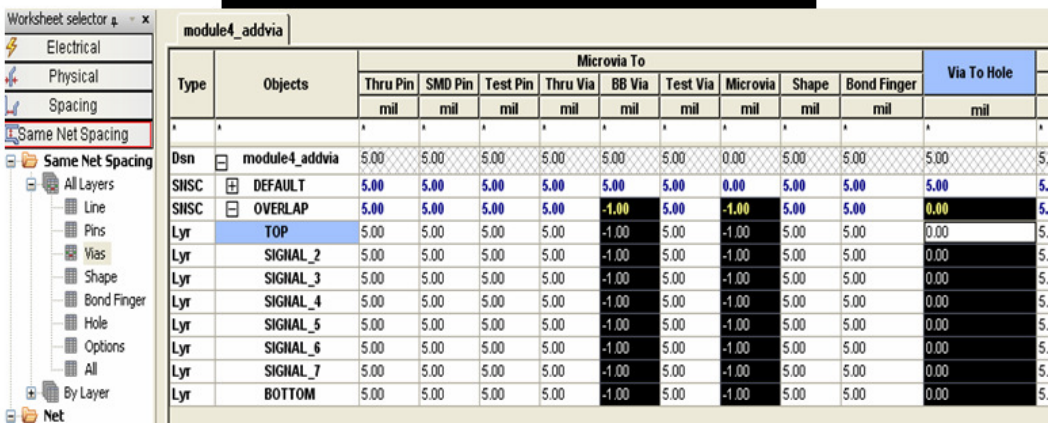
Type	Objects	Vias	BB Via Stagger Min mil	BB Via Stagger Max mil	Allow Etch	Allow Ts	Allow Pad-Pad Connect
*	*	*	*	*	*	*	*
Dsn	⊟ module4_addvia	BB1-2:BB2-3:BB-CORE3-...	0.00	20.00	TRUE	ANYWHERE	VIAS_PINS_O...
PCS	⊞ DEFAULT	BB1-2:BB2-3:BB-COR...	0.00	20.00	TRUE	ANYWHERE	VIAS_PINS_...
PCS	⊞ OVERLAP	BB1-2:BB2-3:BB-COR...	0.00	20.00	TRUE	ANYWHERE	VIAS_P...
PCS	⊞ STACKED_UVIAS_ONLY	BB1-2:BB2-3:BB-COR...	0.00	20.00	TRUE	ANYWHERE	VIAS_P...
PCS	⊟ STACK_ALL	BB1-2:BB2-3:BB-COR...	0.00	20.00	TRUE	ANYWHERE	VIAS_P...
Lyr	TOP		0.00	20.00	TRUE	ANYWHERE	VIAS_PINS_O...
Lyr	SIGNAL_2		0.00	20.00	TRUE	ANYWHERE	VIAS_VIAS_O...
Lyr	SIGNAL_3		0.00	20.00	TRUE	ANYWHERE	VIAS_VIAS_O...
Lyr	SIGNAL_4		0.00	20.00	TRUE	ANYWHERE	VIAS_VIAS_O...
Lyr	SIGNAL_5		0.00	20.00	TRUE	ANYWHERE	VIAS_VIAS_O...
Lyr	SIGNAL_6		0.00	20.00	TRUE	ANYWHERE	VIAS_VIAS_O...
Lyr	SIGNAL_7		0.00	20.00	TRUE	ANYWHERE	VIAS_VIAS_O...
Lyr	BOTTOM		0.00	20.00	TRUE	ANYWHERE	VIAS_PINS_O...

Example 4 – Adding Inset Vias

The following vias are used in sequence (BB1-2, BB2-3, BB3-6, BB6-7, BB7-8) however in this example, rules permit the overlapping of adjacent vias.

- While routing on Layer Top (1), a LMB double-click produces the Via Popup GUI where Layer Bottom (8) is selected.
- BB1-2 is inserted at the pick location; BB2-3 floating on cursor overlapping BB1-2.
- Separation of vias is controlled by the Same Net rule of -1 between via types in combination of Via to Hole rule set to 0. It's the Via to Hole rule that controls the separation between the edge of the via pad and edge of hole.
- The Via to Hole constraint of 0 allows the tangent condition between the vias (pad edge to hole edge)
- The -1 entry bypasses the same net check in favour of the Via to Hole check. If not for the -1 entry, a same net v-v DRC would be produced by the overlap.
- Remaining vias are added sequentially





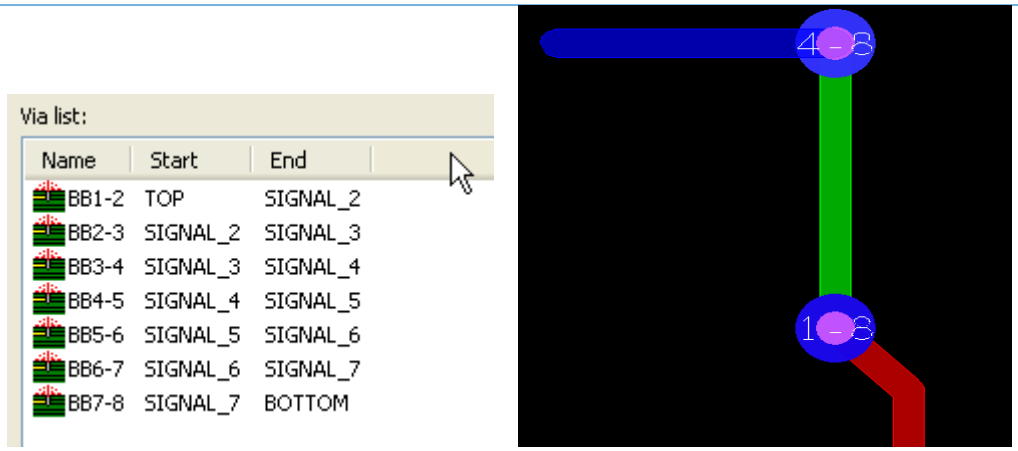
Type	Objects	Microvia To									Via To Hole
		Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Microvia	Shape	Bond Finger	
		mil	mil	mil	mil	mil	mil	mil	mil	mil	mil
Dsn	module4_addvia	5.00	5.00	5.00	5.00	5.00	5.00	0.00	5.00	5.00	5.00
SNSC	DEFAULT	5.00	5.00	5.00	5.00	5.00	5.00	0.00	5.00	5.00	5.00
SNSC	OVERLAP	5.00	5.00	5.00	5.00	-1.00	5.00	-1.00	5.00	5.00	0.00
Lyr	TOP	5.00	5.00	5.00	5.00	-1.00	5.00	-1.00	5.00	5.00	0.00
Lyr	SIGNAL_2	5.00	5.00	5.00	5.00	-1.00	5.00	-1.00	5.00	5.00	0.00
Lyr	SIGNAL_3	5.00	5.00	5.00	5.00	-1.00	5.00	-1.00	5.00	5.00	0.00
Lyr	SIGNAL_4	5.00	5.00	5.00	5.00	-1.00	5.00	-1.00	5.00	5.00	0.00
Lyr	SIGNAL_5	5.00	5.00	5.00	5.00	-1.00	5.00	-1.00	5.00	5.00	0.00
Lyr	SIGNAL_6	5.00	5.00	5.00	5.00	-1.00	5.00	-1.00	5.00	5.00	0.00
Lyr	SIGNAL_7	5.00	5.00	5.00	5.00	-1.00	5.00	-1.00	5.00	5.00	0.00
Lyr	BOTTOM	5.00	5.00	5.00	5.00	-1.00	5.00	-1.00	5.00	5.00	0.00

Example 5 – Adding "Any layer Vias"

The lamination of conductive areas on each layer to conductive areas on the adjacent layers is commonly referred to as "Any Layer Via" construction. Companies providing this technology include ALIVH from Matsushita and FVSS from Ibiden. This technology is primarily used on small consumer electronic products like cell phones to meet high density routing and board thickness requirements.

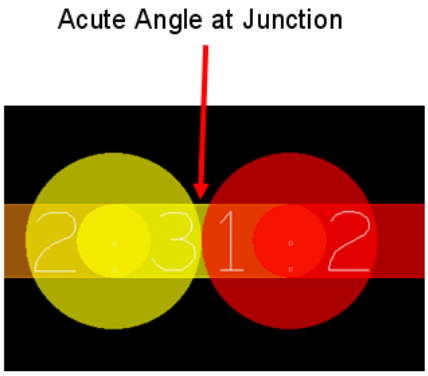
The following vias are used to transition to any layer (BB1-2, BB2-3, BB3-4, BB4-5, BB6-7, BB7-8).

- While routing on Layer Top (1), a LMB double-click produces the Via Popup GUI where Layer Bottom (8) is selected.
- The entire range of vias is inserted at the pick point.
- From the Bottom layer, a LMB double-click to Signal_4 is made; the entire stack between this span is added. The via label is indicative of the complete stacked series of vias (4-8)
- Physical CSet rules to allow stacking include:
  - Min BB Stagger set to 0
  - Allow Pad to Pad Connect set to Vias_Vias_only on all layers except Top and Bottom where settings support Via-in-Pad.
- The slide command treats the stacked vias as a single entity. Use the RMB – Split Stack command to slide a specific via of the stack.



Line Fattening between Tangent Vias

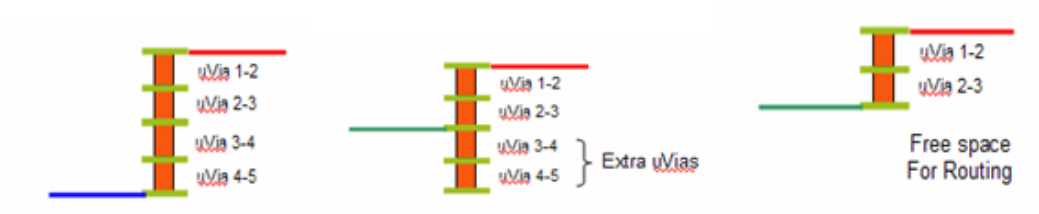
A post route task associated with HDI Design involves increasing the line width between two tangent vias. This is done to remove the acute angle formation between at the junction of the vias.



A post route utility is available to fatten lines between vias based on a user defined edge to edge clearance. The algorithm determined the line width based on the smaller of the two vias. Options are available to 'waive' impedance or max line width DRCs that may result. Users are advised to run this utility near the end of the design process as it's not possible to perform a reset of line width.

Elimination of Unused B/B Vias in Stack

Often vias in a stack may become orphaned as a result of changes made during routing or clip-boarding. The end result leaves unwanted vias that occupy valuable routing real-estate and also contribute to stub effects on the signal.



Trace routed from L1 to 5 | Trace moved to L3 | 2 uVias removed

Unused B/B Via Report

This new report detects unused Buried or Blind vias included in a stack. The removal of these vias can open up routing real estate and reduce stub effects at the via site.

The report is located in **Tools – Reports** and **called Unused Blind/Buried Via Report**

Dynamic Pad Suppression

The removal of unused inner layer pads has traditionally been used to reduce capacitance effects at each hole site. The fabricator's CAM department would be responsible for this application prior to film generation. Possibly the OEM removed the pads as a function of the artwork generation process.

With the ever increasing demand to make product smaller, lighter and cheaper, unused inner layer pads are being removed not only for electrical effects but for physical. Specifically, by removing pads, higher routing densities are achieved by allowing traces to be closer to the edge of the hole.

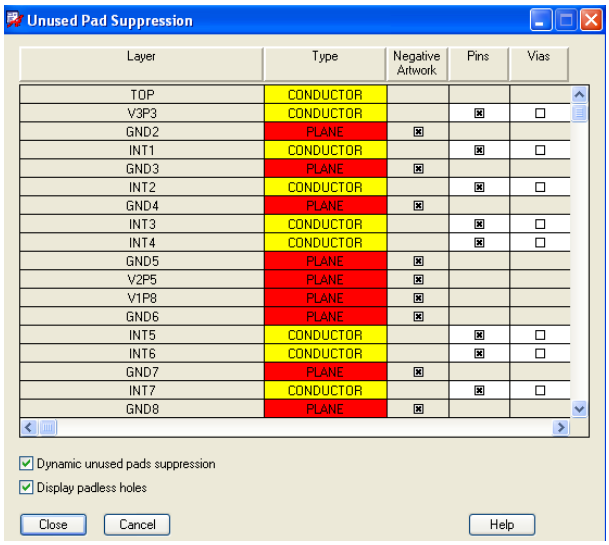
High temperature, lead free soldering has a requirement of leaving pads on unconnected thru pins, but not on unconnected vias. This application is not only object based (pin vs via) but also layer based as to retain the pads on thru pins on the signal layers that are closest to the surface layers.

User Interface

The Pad Suppression User Interface is located in the Setup menu. Each layer of the stack-up is represented; conductor in yellow, planes in red. Settings for Pins and Vias are available and can be enabled on a per layer basis. A **RMB – Enable All Layers** function enables all layers under either the Pin or Via category. Enabling the Dynamic Unused Pads Suppression function automatically enables the display of padless holes.

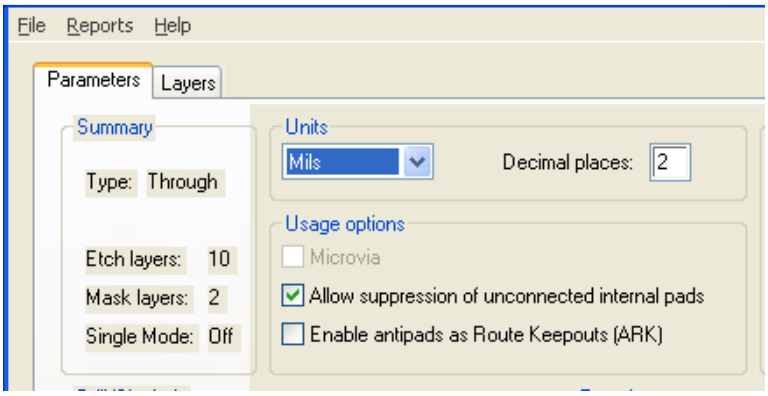
Layer Restrictions

Layers not available for pad suppression include the Top and Bottom Layers, Negative planes and the begin/end layers of a B/B via. The UI will display outer and plane layers for reference only.



Other Restrictions

- Pads associated with Mechanical Pins are not eligible for removal
- Pad Definition must have option “Allow Suppression of unconnected internal pads” enabled for a pad to be consider eligible for removal.



Dynamic Suppression

Pad suppression becomes dynamic once the ‘dynamic unused pad suppression’ option is enabled and form closed. At this point, suppression or restoration is done on the fly. Upon closing the form, all eligible pads are suppressed. From this point forward, pads will be restored as connections are made to pins or vias. In contrast, pads will be dynamically suppressed if traces are deleted from pins or vias.

Disabling the dynamic option will restore all pads on pins and vias. This may result in DRCs if traces are being pushed closer to the drill hole. The next module covers the new drill to metal DRCs.

It should be noted that the pad definition is not altered as a result of suppression.

Exception Properties

- The Unused_pads_ignore property prevents pad suppression at the symbol, net, pin or via element level. Once applied, pads remain static on the respective elements.
- The Unused_pads_override property is used to allow pads to be removed on outer layers. The property is restricted to a symbol with values of Top, Bottom or Top:Bottom. Consider using on edge connectors to minimize the amount of gold used during plating.

Property	Values	Apply to
Unused_pads_ignore	True or Off	Symbol, Net, Pin, Via
Unused_pads_override	Top, Bottom, Top:Bottom	Symbols

Artwork Alignment

The legacy film control 'Suppress unconnected pads' checkbox and functionality is still available for use. If the Dynamic Unused Pads Suppression is currently enabled, the checkbox will be shown enabled for ALL films but greyed out and non-editable and the database driven suppression will be performed. If Dynamic Suppression

however is not enabled, the checkboxes will be individually editable as needed and the old legacy suppression will be performed instead.

The legacy suppression has also been enhanced to now properly handle blind/buried vias where the begin/end layer pads must never be suppressed, even if unconnected and on an internal layer.

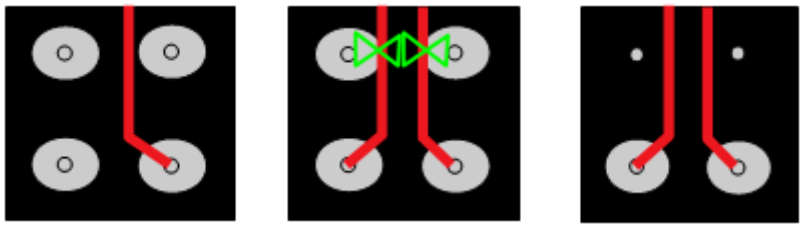
Drill Hole DRC Summary

Drill holes are commonly referred by their plating category; plated or non-plated. The new suite of drill hole checks introduced in 16.2 are based on Allegro pin types (connect pin and mechanical pin). Typically connect pin based holes are plated; mechanical pin based holes non-plated. It is possible in Allegro however to define each type as plated or non-plated. Logic can only be assigned to a connect pin.

The term 'hole' is used in the DRC system and Constraint Manager as the drill hole associated with circuit based pins and vias. Unlike CAM checks were generic PTH to metal checking is performed against minimum constraint values, an integrated CAD system like Allegro must provide the flexibility to check holes against the diverse set of net based rules. For example, if the rules for a 60V net to GND via or pin require a 1mm clearance, this same clearance would be required to the edge of the padless holes associated with these elements.

A 'Hole to Metal' check is performed only when the respective hole is void of pads on conducting layers. This can be a result of 'Null' pad entries in the Padstack definition/instance or the result of using the new pad suppression application. When pads are present on pins and vias, the hole check yields to the convention pin and via checks.

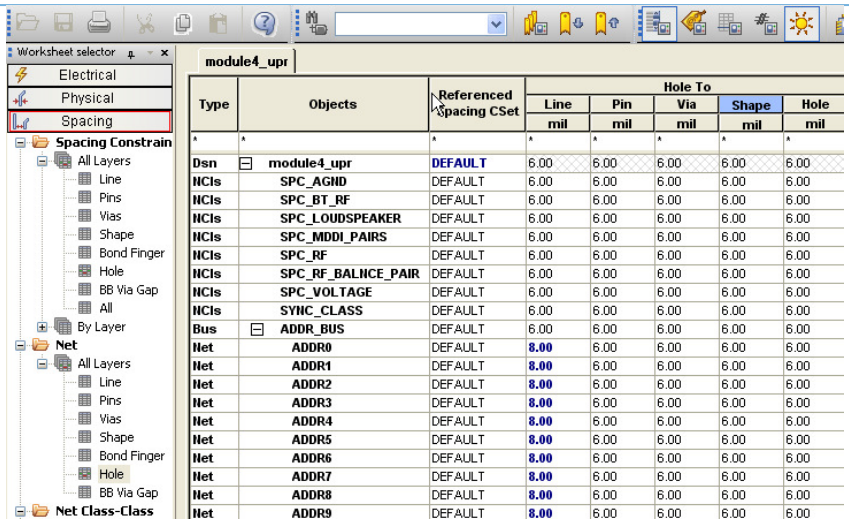
The following example illustrates the potential benefits of drill based checks. The channel width with pads present restricts the number of lines routed between the pin pads to just one. The removal of used pads coupled with a Hole to Line space that permits the line to be routed closer to the edge of the hole but tangent to the annular ring opens up the channel to permit two lines between.



Constraint Manager Integration

Hole to Metal-based constraints can be driven from Spacing CSets or directly set on Net-based objects in Constraint Manager. Both the Spacing and Same Net Spacing Domains support a suite of Hole to (Line, Pin, Via, Shape and Hole) spacing checks. On new boards, Hole-based constraints default to 8 mils; all other spacing constraints default to 5 mils. On uprev'd boards, Hole-based constraints are derived from the Spacing CSets to ensure Metal to Hole spacing is aligned with net spacing rules.

A Hole to Metal DRC is reported when the hole is seen as the outer extent of the pin/via element. If a pad is present and larger than the hole, the spacing DRC uses the pad extents as the geometry to check to. It is not possible to have both a hole and a pin/via pad violation on the same element.



Type	Objects	Referenced Spacing CSet	Hole To: Line (mil)	Pin (mil)	Via (mil)	Shape (mil)	Hole (mil)
*	*	*	*	*	*	*	*
Dsn	module4_upr	DEFAULT	6.00	6.00	6.00	6.00	6.00
NCls	SPC_AGND	DEFAULT	6.00	6.00	6.00	6.00	6.00
NCls	SPC_BT_RF	DEFAULT	6.00	6.00	6.00	6.00	6.00
NCls	SPC_LOUDSPEAKER	DEFAULT	6.00	6.00	6.00	6.00	6.00
NCls	SPC_MDDI_PAIRS	DEFAULT	6.00	6.00	6.00	6.00	6.00
NCls	SPC_RF	DEFAULT	6.00	6.00	6.00	6.00	6.00
NCls	SPC_RF_BALNCE_PAIR	DEFAULT	6.00	6.00	6.00	6.00	6.00
NCls	SPC_VOLTAGE	DEFAULT	6.00	6.00	6.00	6.00	6.00
NCls	SYNC_CLASS	DEFAULT	6.00	6.00	6.00	6.00	6.00
Bus	ADDR_BUS	DEFAULT	6.00	6.00	6.00	6.00	6.00
Net	ADDR0	DEFAULT	8.00	6.00	6.00	6.00	6.00
Net	ADDR1	DEFAULT	8.00	6.00	6.00	6.00	6.00
Net	ADDR2	DEFAULT	8.00	6.00	6.00	6.00	6.00
Net	ADDR3	DEFAULT	8.00	6.00	6.00	6.00	6.00
Net	ADDR4	DEFAULT	8.00	6.00	6.00	6.00	6.00
Net	ADDR5	DEFAULT	8.00	6.00	6.00	6.00	6.00
Net	ADDR6	DEFAULT	8.00	6.00	6.00	6.00	6.00
Net	ADDR7	DEFAULT	8.00	6.00	6.00	6.00	6.00
Net	ADDR8	DEFAULT	8.00	6.00	6.00	6.00	6.00
Net	ADDR9	DEFAULT	8.00	6.00	6.00	6.00	6.00

Hole to Metal DRCs

Design Level Mechanical Pin Spacing DRCs

Mechanical Pins are non-logical elements, typically used to represent mounting/tooling holes and fiducials. Manually drawn keepout areas are normally attached to the Mechanical symbol to restrict etch around the perimeter.

Two Design level checks were provided in release 16.2:

- Mechanical Pin to Mechanical Pin spacing
- Mechanical Pin to Conductor spacing

A new pad usage option permits the antipad associated with the padstack of the Mechanical Pin to be used as an implicit route keepout area. If the pad option is not enabled, the system will revert to the Hole to Metal checks discussed in the previous section. In most cases, it is expected the route keepout areas associated with your current library symbols will prevail in the near term. Going forward, the Mechanical Pin to Conductor spacing DRC provides opportunity to eliminate manually drawn keepout shapes from your library development process as it applies to Mechanical symbols. (.bsms) The Mechanical Pin to Mechanical Pin Spacing DRC can be used to check adjacent Mechanical Pins where antipads are not present in the pad definition. Use the Design Option clearance setting to setup minimum spacing criteria at the global level.

Important – Mechanical Pin checks require the enablement of the pad usage option “Enable antipads as Route Keepouts – ARK)

Modes

DRC modes for holes associated with circuit pins and vias to other metal elements are located in both the Spacing and Same Net Spacing categories. The drill hole is represented as ‘Hole’ in the constraint forms. Hole should be regarded as finished drill hole after plating, not actual drill tool used to drill the hole.

Mechanical Hole-based checks are located in the Design Modes Tab with optional clearance settings in Design Options.

Access these mode settings in **Constraint Manager – Analyze – Analysis Modes**.

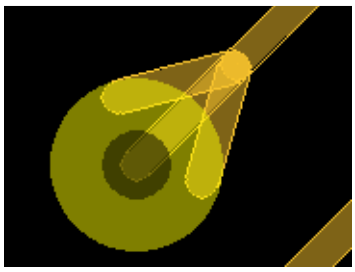
DRC	Spacing	Same Net Spacing	Design Level	Error Code	Comments
Hole to Line	X	X		D-L	On new boards, hole to metal based constraints default to 8 mils
Hole to Pin	X	X		D-P	Metal used to represent pin, via, shape, line
Hole to Via	X	X		D-V	
Hole to Shape	X	X		D-S	Dynamic shapes will void to edge of drill hole
Hole to Hole	X	X		D-D	
Mechanical Hole to Mechanical Hole			X	D-D	Enable padstack option “enable antipads as route keepouts” Violations detected when antipads associated with adjacent holes are null or less than hole size.
Mechanical Hole to Conductor			X	P-L P-V P-S P-P	Enable padstack option “enable antipads as route keepouts” Unique markers for each metal type Consider for future symbol development, eliminates need to draw shapes on mech symbols. Consider for Fiducials

Dynamic Filleting

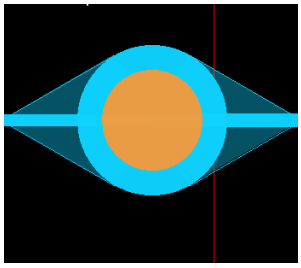
The Gloss-based Fillet application has been enhanced to support the dynamic updating of fillets on pins, vias or T-junctions. The application continues to support the Interactive or Batch mode options as well as the parameters in place. The new dynamic option offers the convenience of filleting during interactive etch editing with no additional procedural steps. When this option is enabled, fillets are added when a connection is made to an element or deleted when removed.

Shape-based Fill

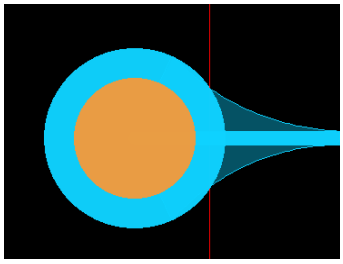
The fill associated with Fillets has transitioned from Line to Shape-based. A single entity fillet is managed more efficiently in the database. For DRC considerations, the fillet should be regarded as an extension of the pin or via.



Line-based Fillet



Shape-based Straight Fillet

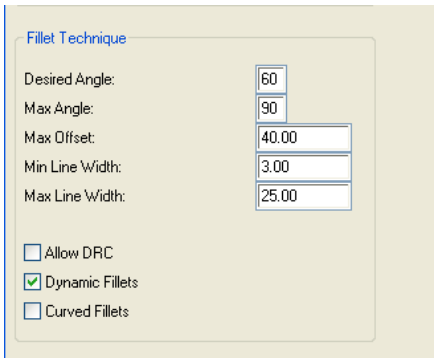


Shape-based Curved Fillet

Enhancements

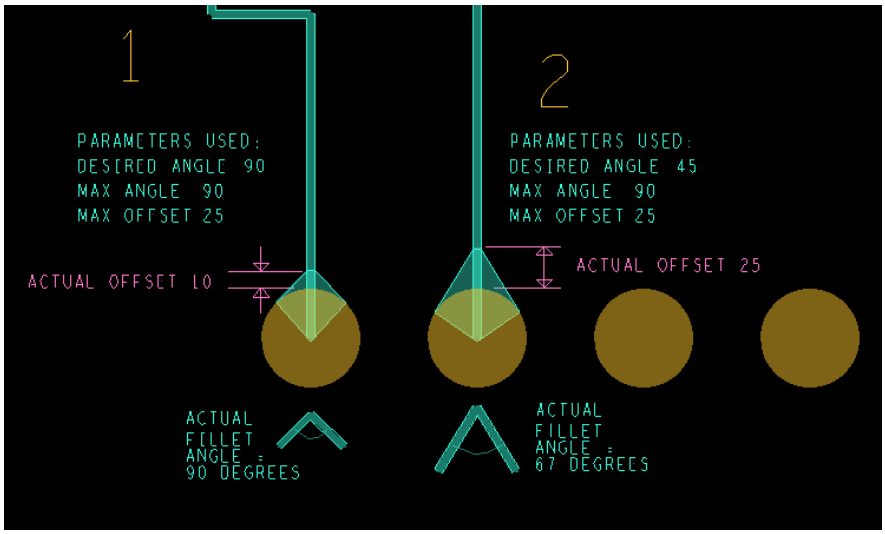
New parameters associated with the Fillet application include:

- Allow DRCs – Fillets can be created with DRCs
- Dynamic Fillets – When enabled, design is updated per parameter settings; fillets are then automatically added/deleted during design editing.
- Curved Fillets – Enable to add curved style fillets; algorithm determines radius
- Max Line Width – Enable to prevent fillets from be added when junction line width is equal to or greater than this value.



Fillet Algorithm

The algorithm first tries to create the fillet at the desired angle, tangent to the pad. If the fillet cannot be created, the angle is incremented up to the Max Angle. If the fillet length, pad tip to vertex of fillet, is greater than the Max Offset, the vertex is adjusted by an amount to satisfy the Max Offset requirement. The end points of the fillet are adjusted by the same amount to maintain the angle.



Reporting

A new report called **Missing Fillets Report** lists junctions with missing or partial fillets. This report can be found in *Tools – Reports* **or** *Tools – Quick Reports***.**

Missing Fillets

Net	Item	Location	Subclass	Partial
AD31	SYMBOL PIN	(3993.00 10264.00)	TOP	
C_BE_L3	SYMBOL PIN	(3993.00 9828.00)	TOP	yes
P66_AD34	VIA	(1925.13 6446.81)	TOP	
P66_AD36	SYMBOL PIN	(1850.00 6425.00)	TOP	
P66_AD36	T	(1847.00 6429.00)	TOP	
P66_AD47	VIA	(1826.00 6600.00)	LAYER_5	yes
P66_IRQ_L4	VIA	(2795.00 6496.00)	LAYER_6	yes
P66_TCK	SYMBOL PIN	(1000.00 11050.00)	LAYER_3	yes
TP_HP_SIC	SYMBOL PIN	(1850.00 6325.00)	TOP	

Exception Property

- The No_Fillet property prevents Fillets from being added at the net, pin or via level. This applies to all layers of the respective element.

Property	Values	Apply to
No_Fillet	True or Off	Net, Pin, Via