

Using OrCAD Capture CIS with PSpice TestBench

Introduction

TestBench enables users of OrCAD Capture CIS and PSpice to extract part of their design and run simulations, make changes to the testbench and then run a difference report between the master design and the testbench. If changes are found you also have the ability to merge the changes back to the master design. This can be ideal especially if you are fine tuning a resistor value as the following example demonstrates.

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Open the required OrCAD Capture PSpice project (ensuring that the project type is of type Analog or Mixed A/D). Once the design is open select the filename.dsn in the Project Window then use Tools – Test Bench – Create Test Bench. Specify a name for the Test Bench and click OK. A new Testbenches area is added at the bottom of the Project structure.



The next step is to open the newly created TestBench. To do this double click the TestBench name in the project window. The TestBench Project will open. This contains a complete copy of the design now named as the TestBench name you specified earlier. You will notice that all the parts in the TestBench design are greyed out. In most cases you will not wish to simulate the complete design, only certain sections of it. The next step is to activate the sections you wish to simulate. Open the relevant pages, select the required parts and use RMB (right mouse button) – TestBench – Add Parts to self. The selected parts will be shown in their default colour scheme.

Using OrCAD Capture CIS with PSpice TestBench			
· · · · · · · · · · · · · · · · · · ·	Import Model Parameters		
Bandpass Filter	Link Database Part	Ctrl+L	
	View Database Part	Ctrl+D	
	Descend Hierarchy		
	Connect		
G1 .	Connect to Bus		
in IN+OUT+ IN+OUT+	User Assigned Reference	+	
IN- OUT-	Lock		
GFREQX	UnLock		
0,-40,180 U 45Meg,-5,90 100Meg,-40,-170	SI Analysis	+	
	TestBench	•	Add Part(s) To Self
150 25Meg -40 170 55Meg -5 -90 500Meg -40 -180	Add Part(s) To Group	Ctrl+Shift+A	Remove Part(s) From Self
	Remove Part(s) From Group	Ctrl+Shift+R	
U	Assign Power Pins		
40Meg,-25,150 60Meg,-25,-150	Ascend Hierarchy		
	Selection Filter	Ctrl+I	

The next step is to check for the floating nets of the selected parts in the Testbench. This step is required because when you activate only a portion of the design, many nets will not be terminated and hence will give floating net errors while running simulations. You can easily resolve this problem by running a floating net search and then terminating the floating nets. To do this select the filename.dsn in the project window then select the dropdown arrow next to the Find binoculars and select Floating Nets option as shown in the figure below. After this click the search button with the binocular shape.

OrCAD Capture CIS-(/BANDPASS_FILTER1 - (FSK2B : PAGE1))		- 8
File Design Edit View Tools Place PCB SI Analysis PSpice Accessories (ptions Window Help CBWare	cāde
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testbench.opj * × /BANDPASS_FILTER1 - (FSK2B : PAGE1) ×	tart Page × / /TEST_SOURCE1 - (FSK1 : PAGE1) × / /TEST_SOURCE1/VCO1 - (FSK11 : PAGE1) × / /TEST_SOURCE1/SUMMER1 - (FS	(13 : PAGE1) × //TEST_SOURCE1/AC1 - (FSK15 : PAGE1) × Find + :
Analog or Mixed A/D	4 3	2
The R. Hierarchy		Find what:
Design Resources		· · · Find
ATestBench.dsn		Find in:
B - D FSK		Parts Differential Pair
E-C FSK1	Dendroes Filter	Part Pins Physical CSet
PAGET p	Danopass Filter	Hierarchical Pine Bectrical CSet
PAGE1		Hierarchical Ports Spacing CSet
B FSK12		Off-Page-Connectors Matched Group
PAGE1		Nets Uass
₽	· · · · · · · · · · · · · · · · · · ·	Rat Nets DBC Medica
In PAGE1	IN+OUT+	Roating Nets
B-C FSK14	IN- OUT-	out out Power/GND Bookmarks
PAGET	GFREQX	Variant Parts
PAGE1	0,-40,180 U 45Meg,-5,90 100Meg,-40,-1	70 Find options:
⊖ C→ FSK2B	R13	S R14
PAGE1		150 Use Regular Expresions
B FSK2T	25Meg,-40,170 55Meg,-5,-90 500Meg,-40,-1	80 Property Name=Value
⊞ C FSK3		• 0 Result options:
	40Meg -25 150 60Meg -25 -150	Highlight
B- PSK32		

Any floating nets will be listed in the Floating Nets tab of the Find Window.

Net Name	Page	Page Number	Schematic	Pin
45MHZ	PAGE1	1	FSK\	DEMODULATOR1.out1
55MHZ	PAGE1	1	FSK\	DEMODULATOR1.out2
N00092	PAGE1	1	FSK\	BANDPASS_FILTER1.out, DEMODULATOR1.in
	Net Name 45MHZ 55MHZ N00092	Net Name Page 45MHZ PAGE1 55MHZ PAGE1 N00092 PAGE1	Net Name Page Page Number 45MHZ PAGE1 1 55MHZ PAGE1 1 N00092 PAGE1 1	Net Name Page Page Number Schematic 45MHZ PAGE1 1 FSK\ 55MHZ PAGE1 1 FSK\ N00092 PAGE1 1 FSK\

For this example we will add the resistor R13 to the TestBench which will effectively give the net a path to ground and resolve any further Floating nets. Use the same steps as before to add the resistor to the TestBench group, you can also re-run the floating nets search to conform you no longer have any floating nets.

We will now add a Voltage source to drive the required simulation. Use Place – PSpice Component – Source – Voltage Sources – AC and add between the IN+ pin of G1 and ground (0).

Using OrCAD) Capt	ure CIS with I	PSpice TestBench		
ERI - (FSIC2B : PAGE1)) Place PCB SI Analysis Part PSpice Component Search Providers Database Part J [®] Wire Auto Wire J [®] Bus 	PSpice Acc	essories Options Window PSpice Ground Capacitor Diode Inductor Resistor Digital	Help CEWare Q Q C Q C Q D I O F 1 (13: PAGE1) × TEST_SOURCE1/ATTENUATOR1 - 9 Band	1Vac 0Vdc	Bandpa:
N Net Alize	E	Discrete Passives		· in · · · · · · · · · · · · · · · · · ·	IN+O
NetGroup NetGroup Yan Power	U	Source	Controlled Sources	· · · · · · · · · · · · · · · · · · ·	040.180 = 0 G 45V
 Ground Off-Page Connector Hierarchical Block Hierarchical Plot Hierarchical Plot 	G	Modeling Application	DC Puise 0,-40 Sine Exponential	R13	25Meg,-40,170 55M
}% No Connect	x	· · · · · · · · · ↓	150 25Me ^{FM Sine} TestBench →	Ū	

We are now ready to run the PSpice simulation. We will start by creating a new simulation profile, PSpice – New Simulation Profile, specify a name AC and click on Create.

New Simulation	×
Name:	Create
Ad	
Inherit From:	Cancel
none *	
Root Schematic: FSK	

Select AC Sweep/Noise as the analysis type and set the values for start/end frequency and points decade as shown below.

Simulation Settings - AC			×
General Analysis Configuration Files Options Data Collection Probe Window	Analysis Type: AC Sweep/Noise	AC Sweep Type Linear Linear Logarithmic Decade Points/Decade: Noise Analysis Enabled Output Voltage: I/V Source: Interval: Output File Options Include detailed bias point information for nonlinear controlled so semiconductors (.OP) OK Cancel Apply Reset	10meg 10G 100

Now add a marker to the OUT- pin of G1. For this example we will use PSpice – Markers – Advanced – db Magnitude of Voltage.





Once the desired results are obtained you can compare the schematics in the master design and test bench to highlight the differences. To do this select the master design filename.dsn in the Project Window and select Tools – Test Bench – Compare Test Bench

OrCAD Capture CIS-[/BANDF	ASS_FIL	ter1 - (f	SK2B :	PAGE1)]					
File Design Edit View	Tools	Place	PCB	SI Analysis		PSpice	Accessories	Reports	Options
	S A	nnotate.				i H	VAC		· 🛱 ,
testbench.opj	 Back Annotate Update Properties 				Page X /TEST_SOURCE1/SUMMER			UMMER1 - (FS	
Analog or Mixe	Te	est Bench	1		Þ	C	reate Test Ben	ch	Shift+B
Design Resources	Create Netlist			Compare Test Bench		Shift+D			
I estBench.dsn	С	reate Dif	ferenti	al Pair		I			

The following window will show the differences between the master design and the test bench. We will select the value of 150 in the master design and update this with the new required value of 250 by selecting the value and then using the Accept Left button.



The Compare window now shows the designs are identical.

Start Page X //BANDPASS_FILIER1 - (FSK28 : PAGE1) X SVS X			
🕞 🖧 🖧 🕜 Design_View 🔹 🔇			
	Object Type/Value	Object	Object Type/Value/Description
view objects are from C:\CADENCE\SPB_17.4\TOOLS\PSPICE\CAPTURE_SAMPLES\MIXSIM\FSK\FSK-TBFiles/FSK/TestBench\TestBench.DSN		Target view objects are from C:\CADENCE\SPB_17.4\TOOLS\PSPICE\CAPTURE_SAMPLES\MIXSIM\FSK\FSK.DSN	
s /BANDPASS_FILTER1	Design_View HIER_INSTANCE		HIER_INSTANCE

The value is updated in the schematic.



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