Using OrCAD Capture CIS with PSpice TestBench

Introduction

TestBench enables users of OrCAD Capture CIS and PSpice to extract part of their design and run simulations, make changes to the testbench and then run a difference report between the master design and the testbench. If changes are found you also have the ability to merge the changes back to the master design. This can be ideal especially if you are fine tuning a resistor value as the following example demonstrates.

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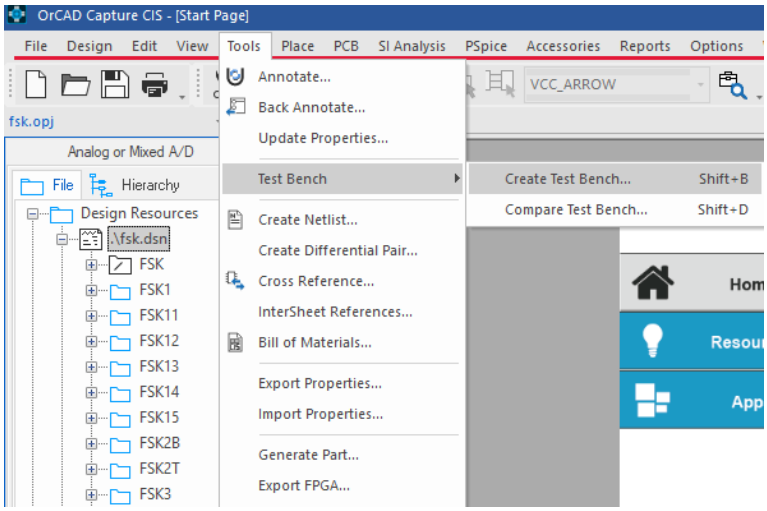
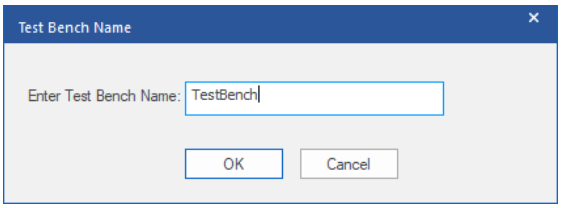
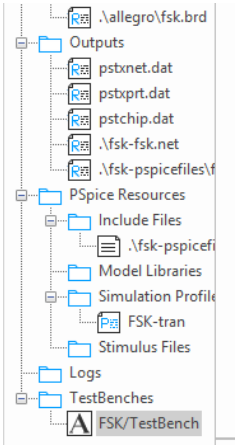
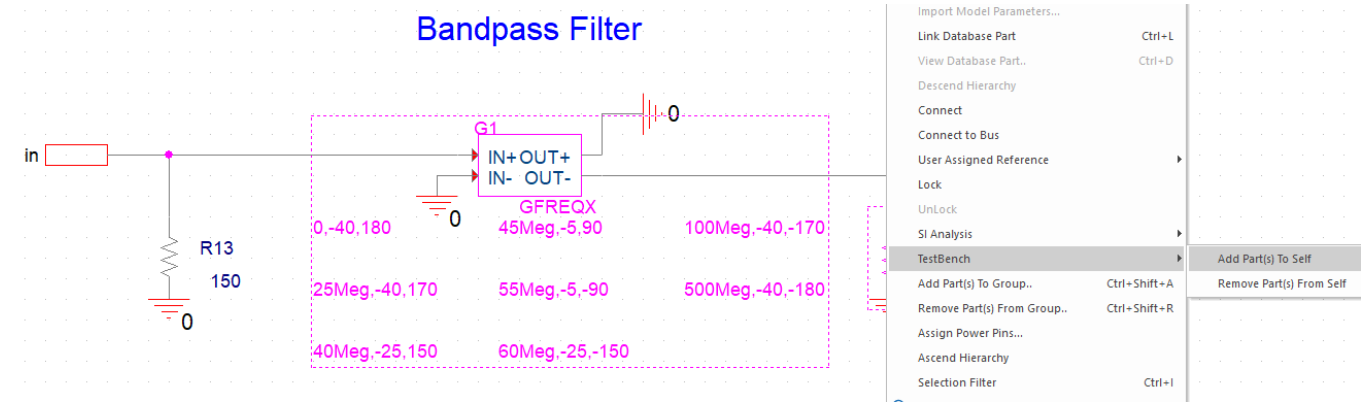
Open the required OrCAD Capture PSpice project (ensuring that the project type is of type Analog or Mixed A/D). Once the design is open select the filename.dsn in the Project Window then use Tools – Test Bench – Create Test Bench. Specify a name for the Test Bench and click OK. A new Testbenches area is added at the bottom of the Project structure.



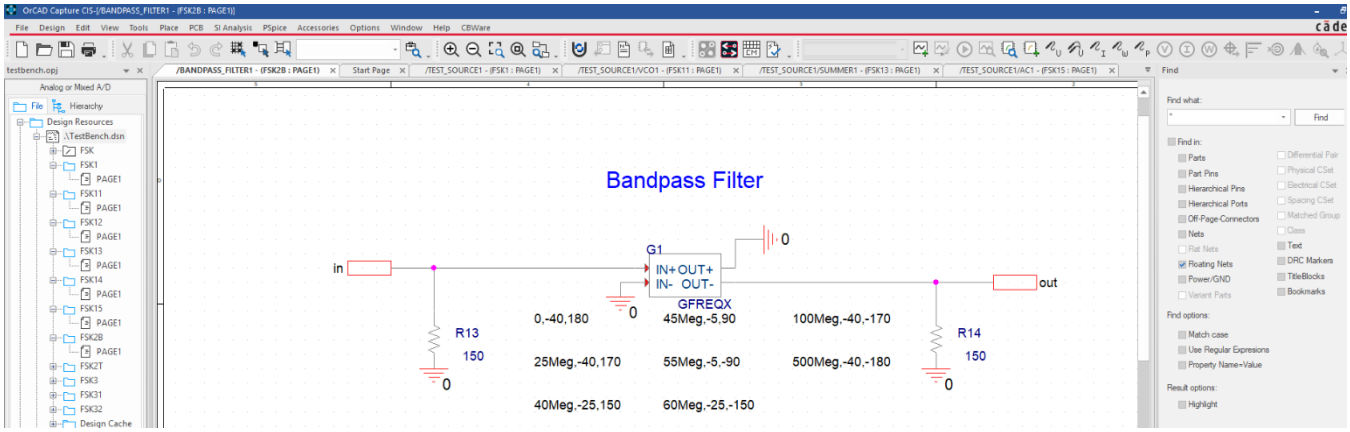




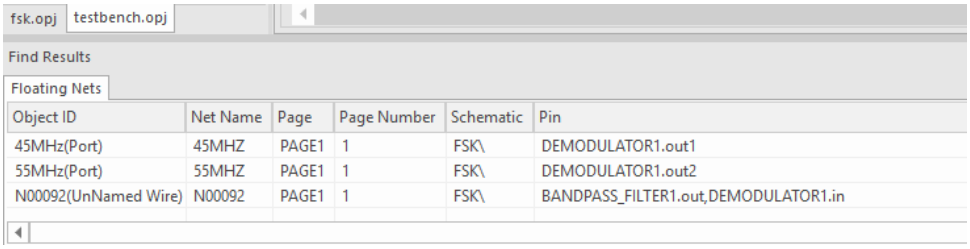
The next step is to open the newly created TestBench. To do this double click the TestBench name in the project window. The TestBench Project will open. This contains a complete copy of the design now named as the TestBench name you specified earlier. You will notice that all the parts in the TestBench design are greyed out. In most cases you will not wish to simulate the complete design, only certain sections of it. The next step is to activate the sections you wish to simulate. Open the relevant pages, select the required parts and use RMB (right mouse button) – TestBench – Add Parts to self. The selected parts will be shown in their default colour scheme.



The next step is to check for the floating nets of the selected parts in the Testbench. This step is required because when you activate only a portion of the design, many nets will not be terminated and hence will give floating net errors while running simulations. You can easily resolve this problem by running a floating net search and then terminating the floating nets. To do this select the filename.dsn in the project window then select the dropdown arrow next to the Find binoculars and select Floating Nets option as shown in the figure below. After this click the search button with the binocular shape.



Any floating nets will be listed in the Floating Nets tab of the Find Window.



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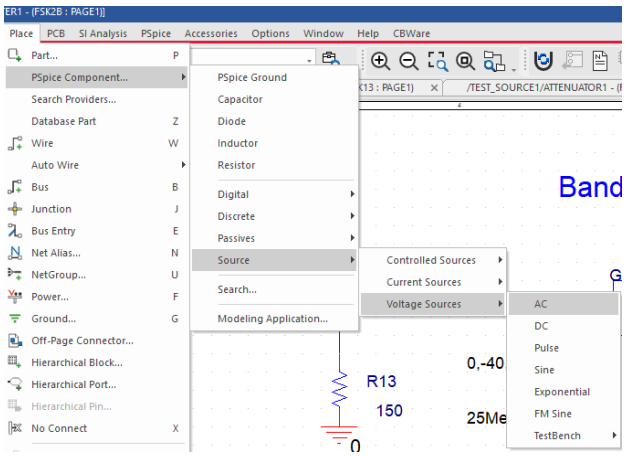
Find Results

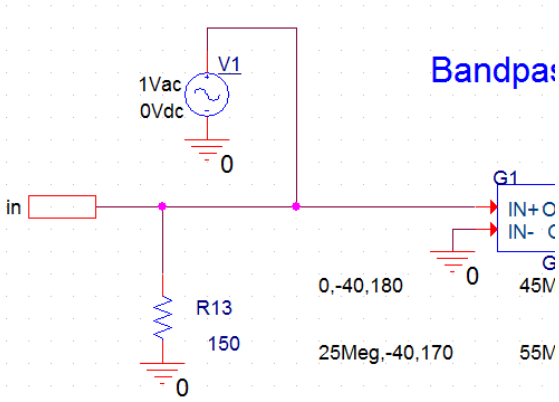
Floating Nets

Object ID	Net Name	Page	Page Number	Schematic	Pin
45MHz(Port)	45MHZ	PAGE1	1	FSK\	DEMODULATOR1.out1
55MHz(Port)	55MHZ	PAGE1	1	FSK\	DEMODULATOR1.out2
N00092(UnNamed Wire)	N00092	PAGE1	1	FSK\	BANDPASS_FILTER1.out,DEMODULATOR1.in

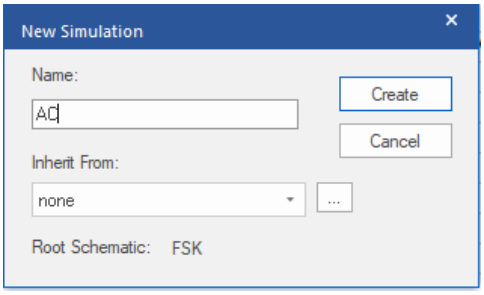
For this example we will add the resistor R13 to the TestBench which will effectively give the net a path to ground and resolve any further Floating nets. Use the same steps as before to add the resistor to the TestBench group, you can also re-run the floating nets search to conform you no longer have any floating nets.

We will now add a Voltage source to drive the required simulation. Use Place – PSpice Component – Source – Voltage Sources – AC and add between the IN+ pin of G1 and ground (0).

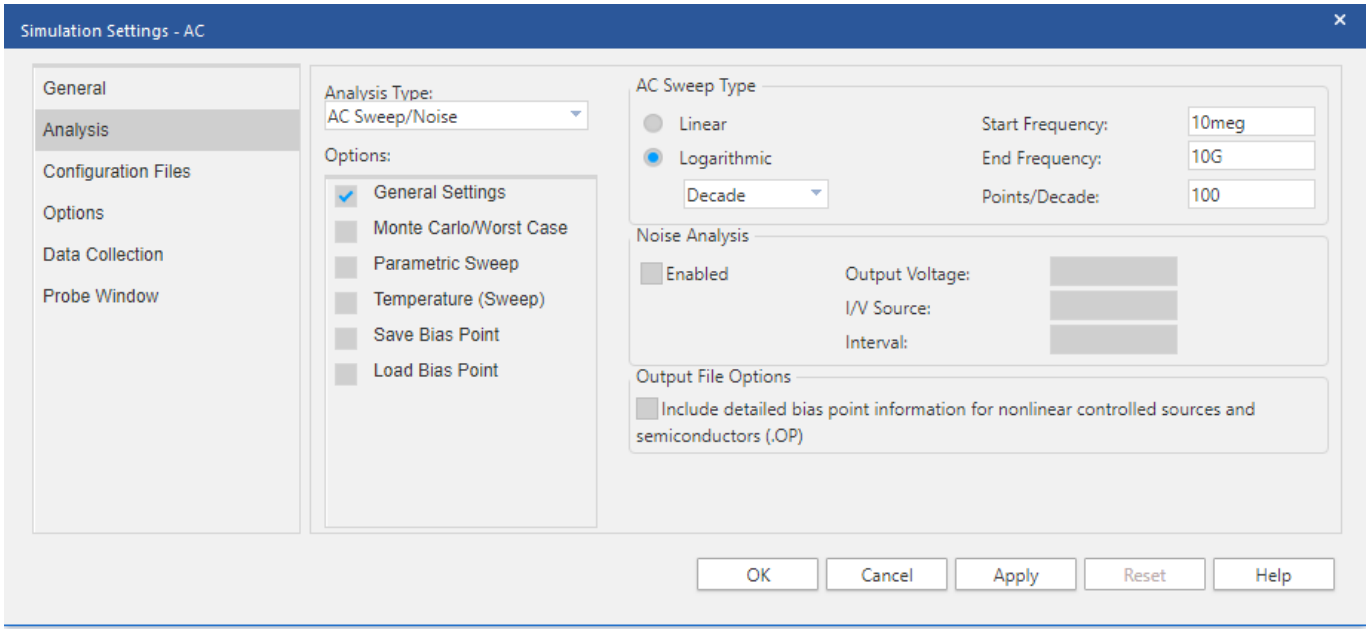




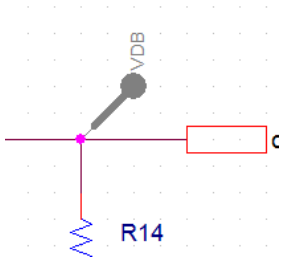
We are now ready to run the PSpice simulation. We will start by creating a new simulation profile, PSpice – New Simulation Profile, specify a name AC and click on Create.



Select AC Sweep/Noise as the analysis type and set the values for start/end frequency and points decade as shown below.

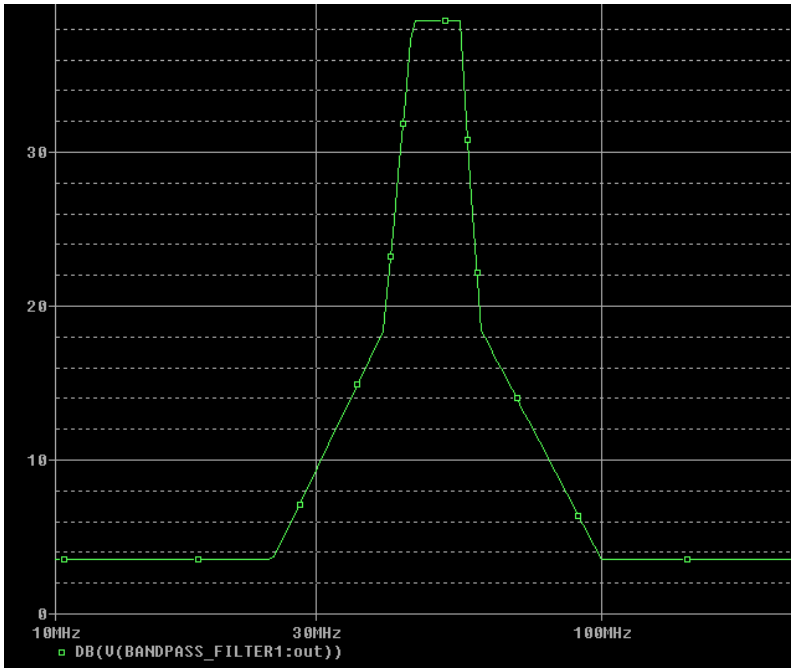


Now add a marker to the OUT- pin of G1. For this example we will use PSpice – Markers – Advanced – db Magnitude of Voltage.

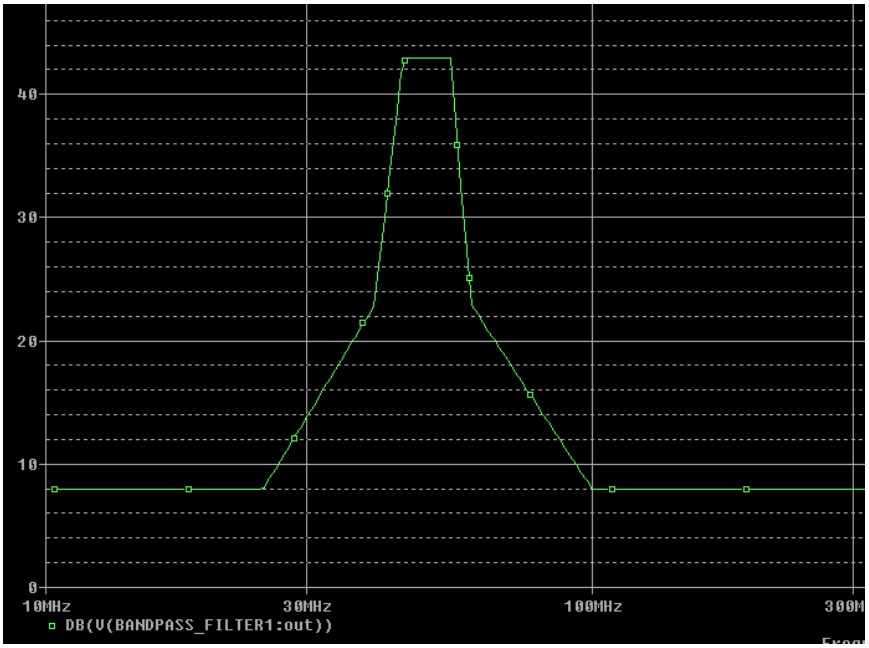


Run the simulation from PSpice – Run or use the run icon 

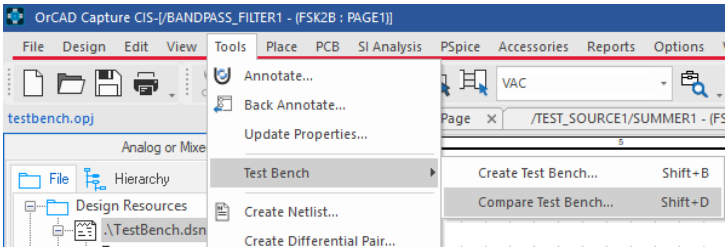
The results are as follows:-



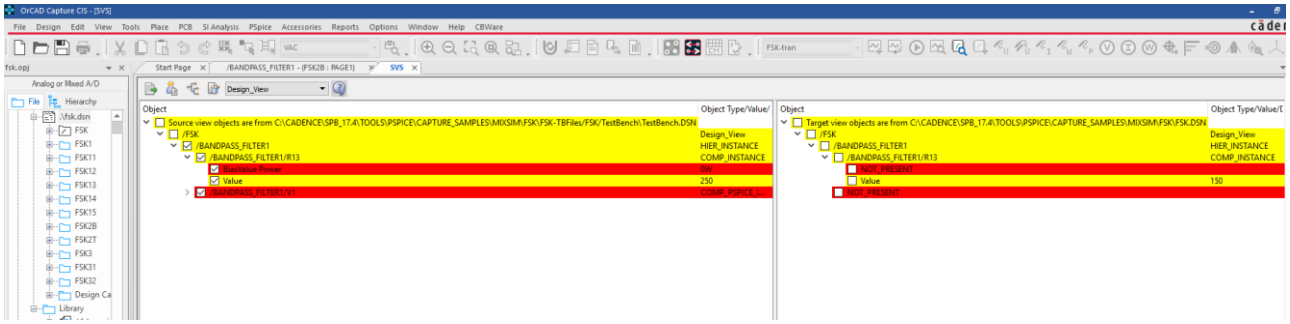
If the desired output does not meet the requirements you can adjust the resistance values and re-run the simulation. In this instance we will change the resistance value of R14 from 150 to 250 ohms resulting in:-



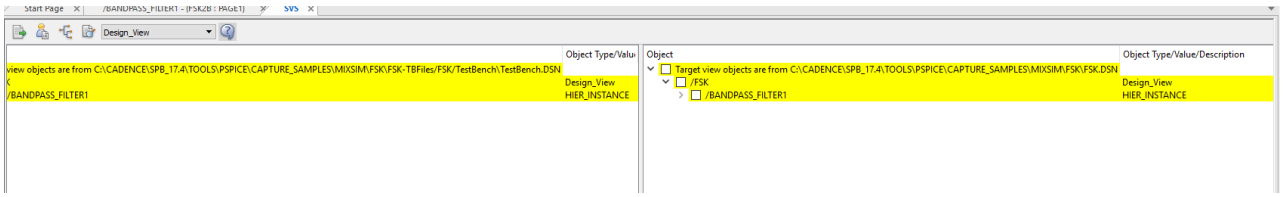
Once the desired results are obtained you can compare the schematics in the master design and test bench to highlight the differences. To do this select the master design filename.dsn in the Project Window and select Tools – Test Bench – Compare Test Bench



The following window will show the differences between the master design and the test bench. We will select the value of 150 in the master design and update this with the new required value of 250 by selecting the value and then using the Accept Left button. 



The Compare window now shows the designs are identical.



The value is updated in the schematic.