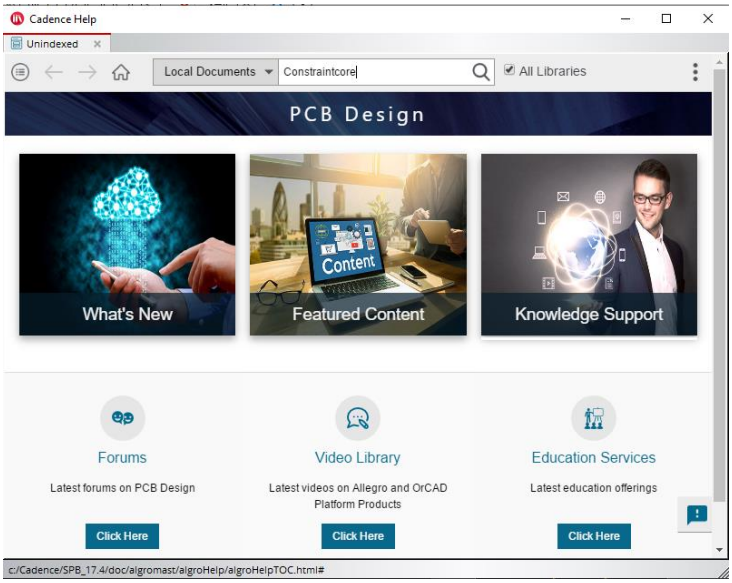
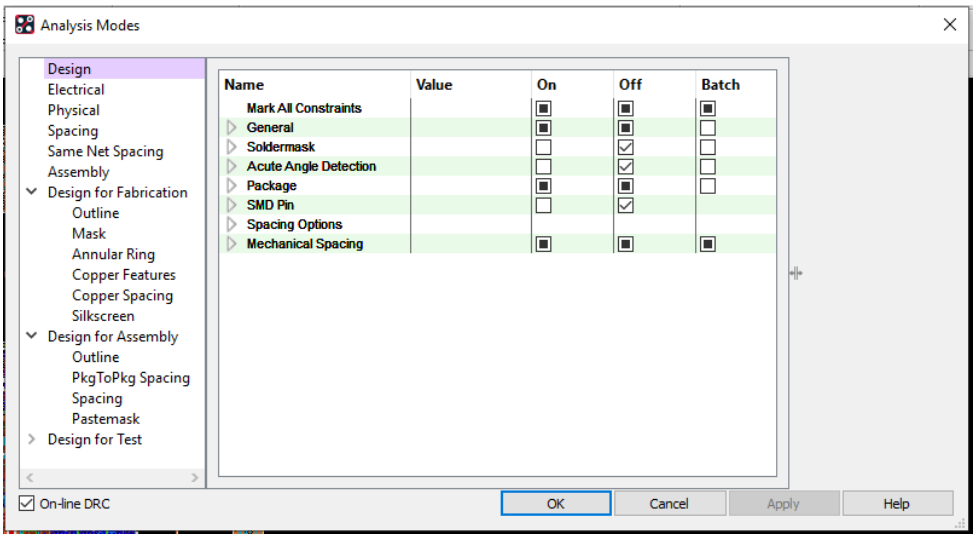
Constraint Modes in OrCAD and Allegro PCB Designer

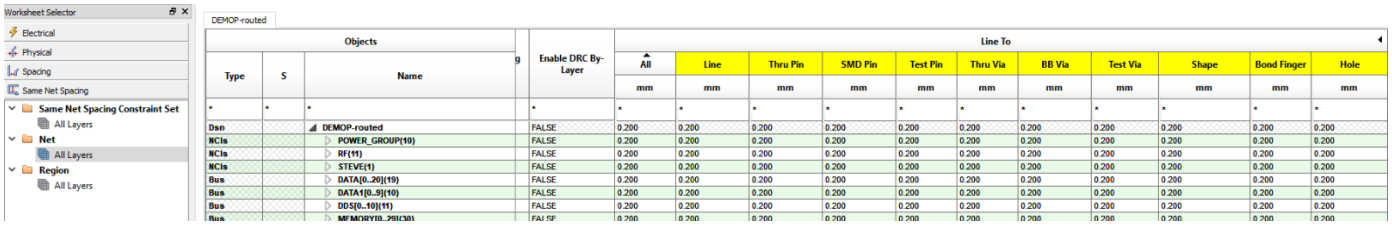
The Cadence OrCAD and Allegro PCB Design tools have many DRC modes to cover rules such as physical track thickness or spacing rules, same net spacing rules or placement boundary rules to aid with the design of a PCB. Many of these rules are enabled by default when you first invoke the tools but there are also many that need to be enabled to see the required DRC markers. This app note describes how to access and enable / disable the DRC Modes and also a brief explanation of what the rules will do. This note will also describe the different levels of DRC Modes available depending on license availability. For more details of the DRC checks that are referenced in this PDF please launch Help – Documentation (from within PCB Editor) then type Constraintcore followed by a return. From the results choose Allegro Platform Constraints Reference and on the opening page right click anywhere and choose Show PDF.



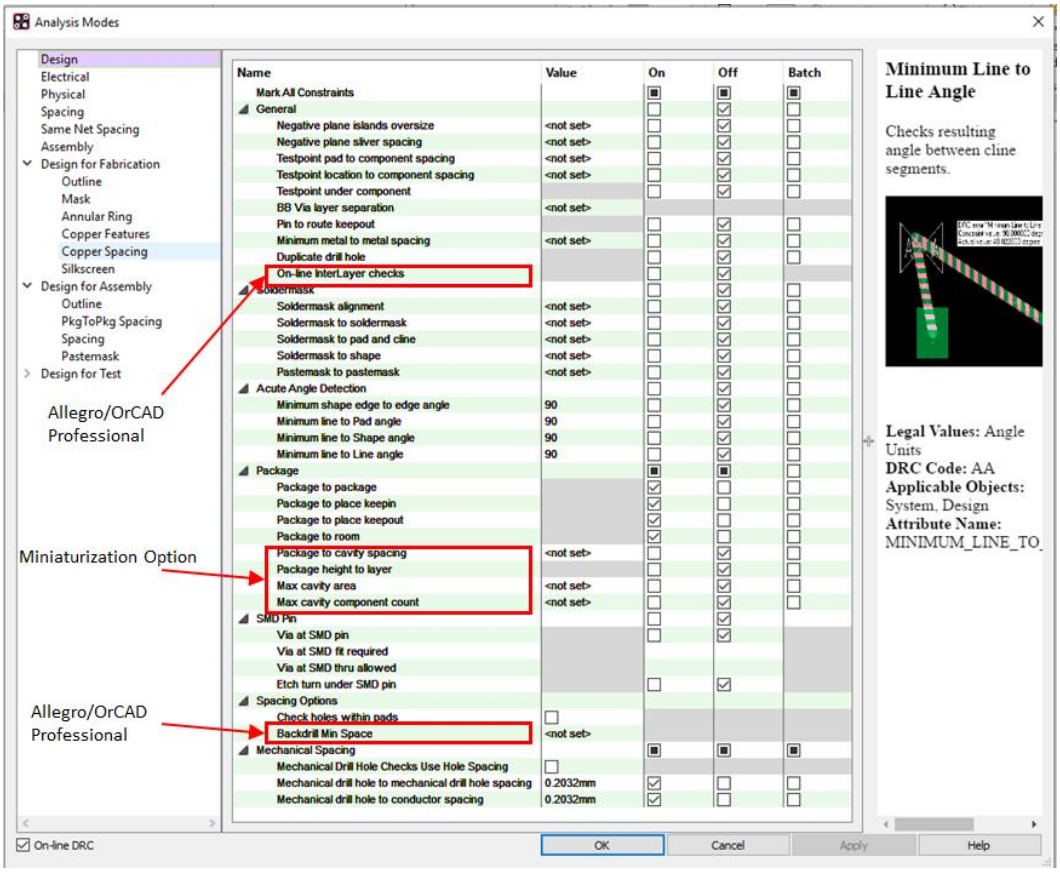
To access the Constraint Modes, you can either use Setup > Constraints > Modes from within Allegro, Setup > Constraint Modes from within OrCAD PCB or from the Constraint Manager Window use Analyze > Analysis Modes to see the Analysis modes GUI.



A useful feature of the Constraint Manager to quickly reference whether a DRC Mode is enabled or not is a colour coded title. An example of this is if you look at the Same Net Spacing - Same Net Spacing Constraint Set – All Layers workbook you will see the available rules. A quick indication that the DRC Modes are not enabled is shown by the Column header being coloured Yellow. You can, either go to the Constraint Modes and enable the DRC's or RMB (right mouse button) on the column header and choose Analysis Mode to quickly turn the rule on.



Design



Negative plane islands oversize - Scales up the pad geometry before the check for Negative plane islands.

Negative plane sliver spacing – Specifies spacing checks for Negative plane sliver spacing.

Testpoint pad to component spacing – Specifies spacing checks between the edges of testpoint pads and components.

Testpoint location to component spacing – Specifies spacing checks between testpoint locations (centre) and components.

Testpoint under component – On/Off check to look for a testpoint located under a Place_Bound shape.

BB Via layer separation – A design-level integer property that specifies the span of layers where the MIN VIA GAP check is applied. By default, the span is infinite, which means that all non-connected vias are checked even if they appear on the opposite sides of the design.

Pin to route keepout – On/Off check to look for a pin within a route keepout area.

Minimum metal to metal spacing – To flag spacing errors that occur when certain spacing modes are accidentally set to OFF, and for CAD<>CAM alignment. It is best to run this check, near design completion. This checked is intended to work as a net to net check; same net behaviour is not supported.

Duplicate drill hole – On/Off check to detect overlapping drill holes.

On-Line InterLayer checks (Allegro/OrCAD Professional) – Enable the Inter layer DRC checks for flexi rigid designs.

Soldermask

Soldermask alignment – Specifies the alignment tolerance required for the proximity of package soldermask to placebound and pad soldermask to pad geometry.

Soldermask to soldermask – Specifies spacing checks for pad soldermask to pad soldermask, symbol soldermask to symbol soldermask and symbol soldermask to pad soldermask.

Soldermask to pad and cline – Specifies spacing checks between the soldermask and pads or clines.

Soldermask to shape – Specifies spacing checks between the soldermask and shapes.

Pastemask to pastemask - Specifies spacing checks for pad pastemask to pad pastemask and pad pastemask to package based pastemask.

Acute Angle Detection

Minimum Shape edge to edge angle – Checks resulting angle between shape segments that are part of the same shape. This angle is created at the outer edges of the shape.

Minimum Line to Pad angle – Checks resulting angle at the point a cline enters a pad.

Minimum Line to Shape angle – Checks resulting angle at the point a cline enters a shape.

Minimum Line to Line angle - Checks resulting angle between cline segments.

Package

Package to Package – Flags packages that overlap one another.

Package to place keepin – Flags packages that extend beyond a place keepin.

Package to place keepout - Flags packages that extend inside a place keepout.

Package to room – Flags packages that are located in rooms to which they are not assigned.

Package to Cavity (Miniaturization Option) – Verifies the clearance between the edges of a package placebound shape to edge of cavity outline. Packages that do not maintain this distance are flagged. The clearance value or the minimum distance between the edge of the placebound shape to the cavity outline is specified in the Package

to cavity spacing field, available in the Design Options page of the Analysis Modes dialog box. The default clearance value is 0.

Package height to layer (Miniaturization Option) - Verifies the spacing between package height and the layer. Checks if the package height is less than the thickness of the layer(s) that the cavity spans.

Max cavity area (Miniaturization Option) – Verifies the maximum cavity area violation.

Max cavity component count (Miniaturization Option) - Verifies the maximum number of components that can reside in the cavity.

SMD Pin

Via at SMD pin – Toggle to enable to the Via in Pad DRC's before

Via at SMD fit required – This constraint is attached to components/component pins, or symbols/symbol pins. Property values are on or off. When on, it specifies that a via is allowed inside an SMD pin, but only if it is completely covered by the pin. When off, just the centre of the via needs to be inside the pin. In cases where the property is attached to a symbol, the property is extended to all instances of the symbol.

Via at SMD thru required – This constraint is attached to components/component pins, or symbols/symbol pins. Property values are on or off. When on, it specifies that a through hole via, blind via, or microvia is allowed inside an SMD pin. When off, only partial vias are allowed. In cases where the property is attached to a symbol, the property is extended to all instances of the symbol.

Etch turn under SMD Pin - When ON this constraint checks multi-segment bends within a pad boundary. The check is limited to nets containing electrical pin-pair constraints.

Spacing Options

Check holes within pads - When On, drill hole checks are run using the drill hole explicitly. The presence of pads associated with the drill hole is not relevant in this mode of the DRC calculation. When Off, the drill-hole checks are run when the pad is suppressed or undefined exposing the bare hole.

Backdrill Min Space (Allegro/OrCAD Professional) - The BACKDRILL_MIN_SPACE property, attached to a drawing, suppresses drill hole DRCs on the backdrill layers by providing a reduced clearance value to the backdrill holes. Ensure that drill hole checks are enabled in the design.

Mechanical Spacing

Mechanical Drill Holes Checks Use Hole Spacing – When On any Mechanical Drill hole will use the Hole to Spacing rules.

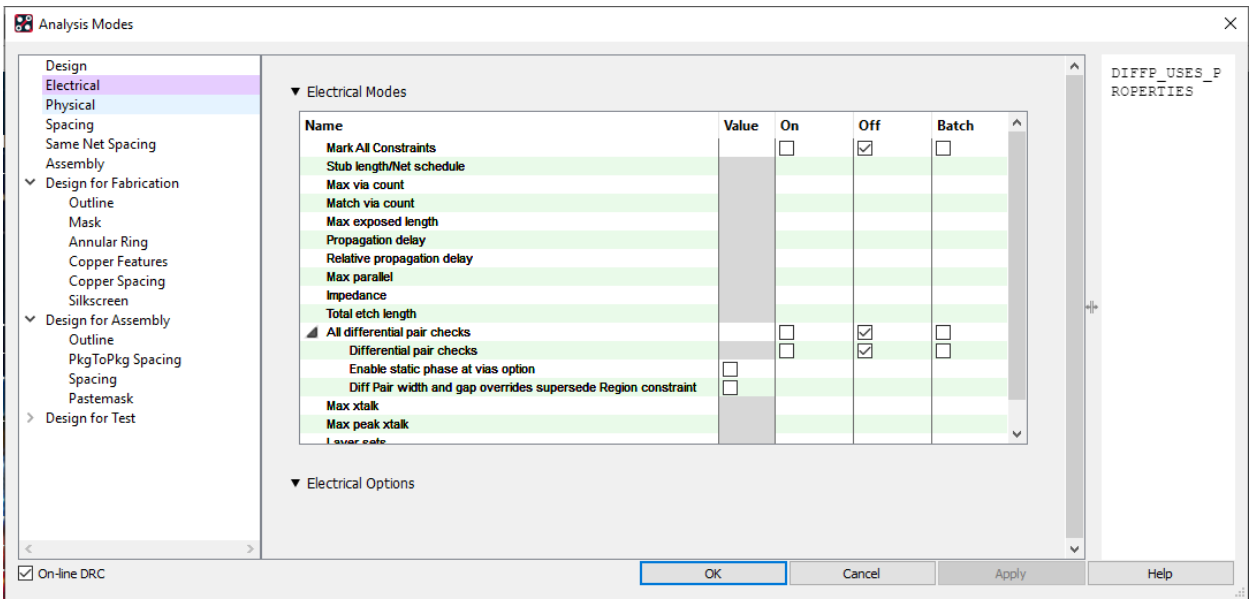
Mechanical drill hole to mechanical drill hole spacing – Specifies spacing checks between mechanical pins.

Mechanical drill hole to conductor spacing - Specifies spacing checks between mechanical pins and conductors.

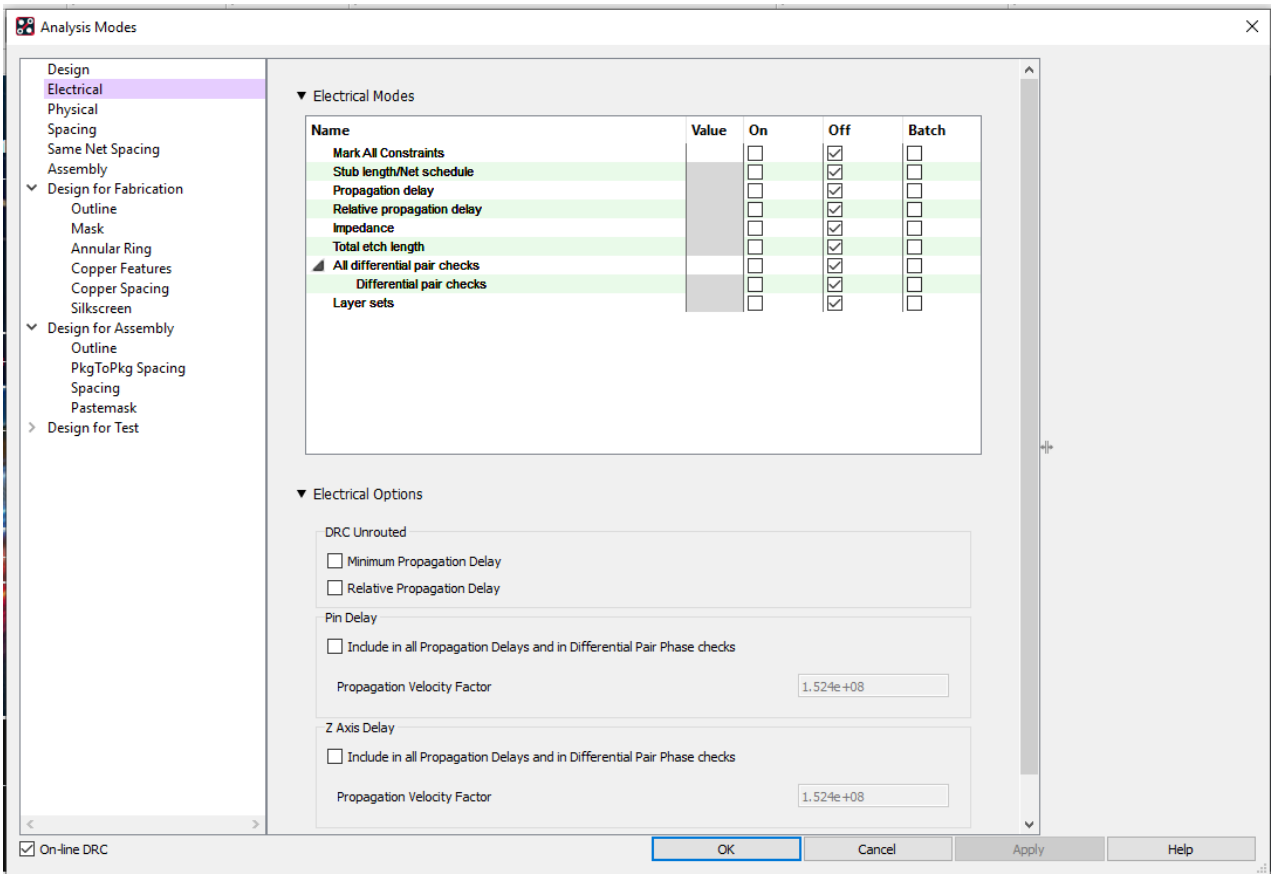
Electrical

The Electrical Constraint Modes are different depending on the license you have. Below are screenshots of OrCAD Standard, Professional, Allegro PCB Designer and + High Speed Options.

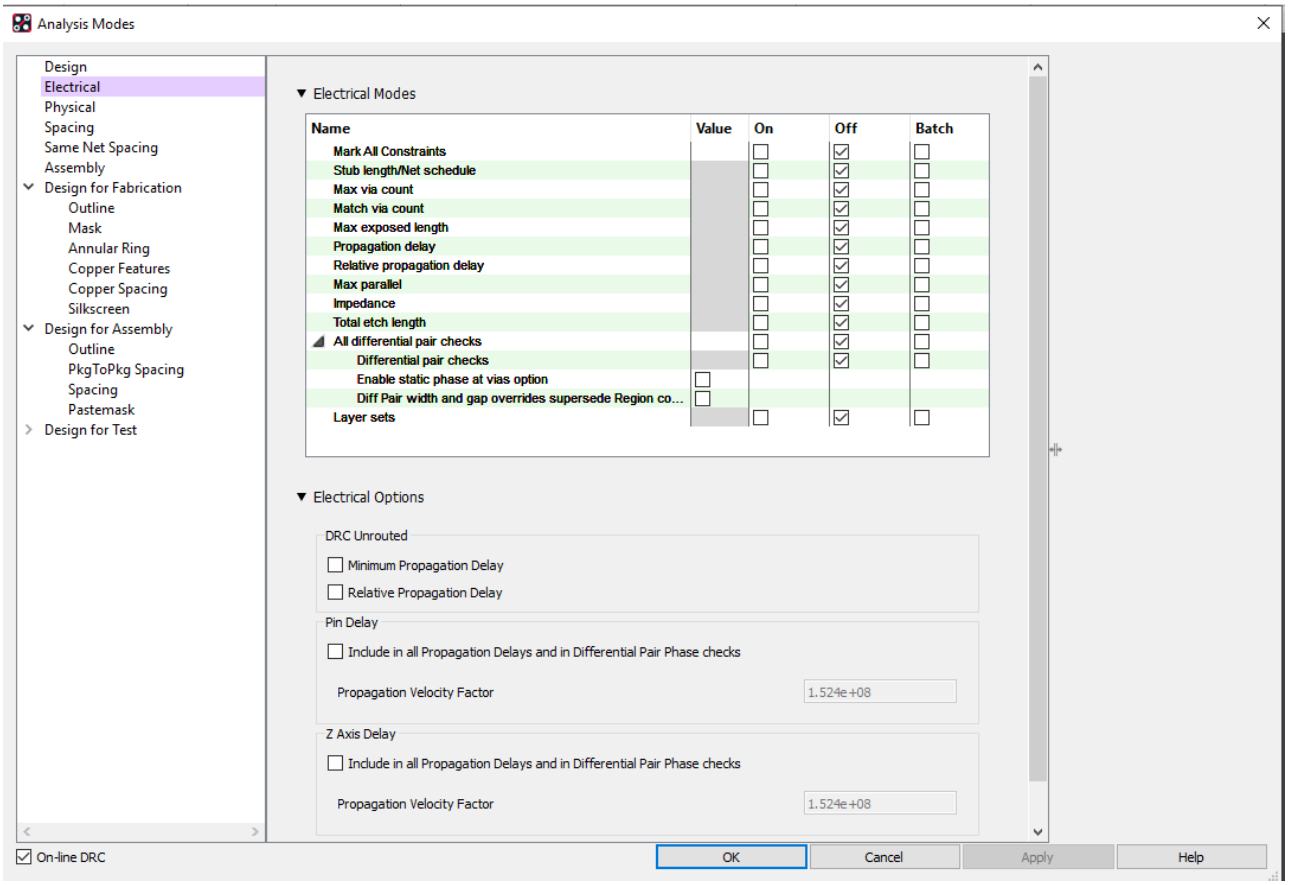
OrCAD PCB Designer Standard



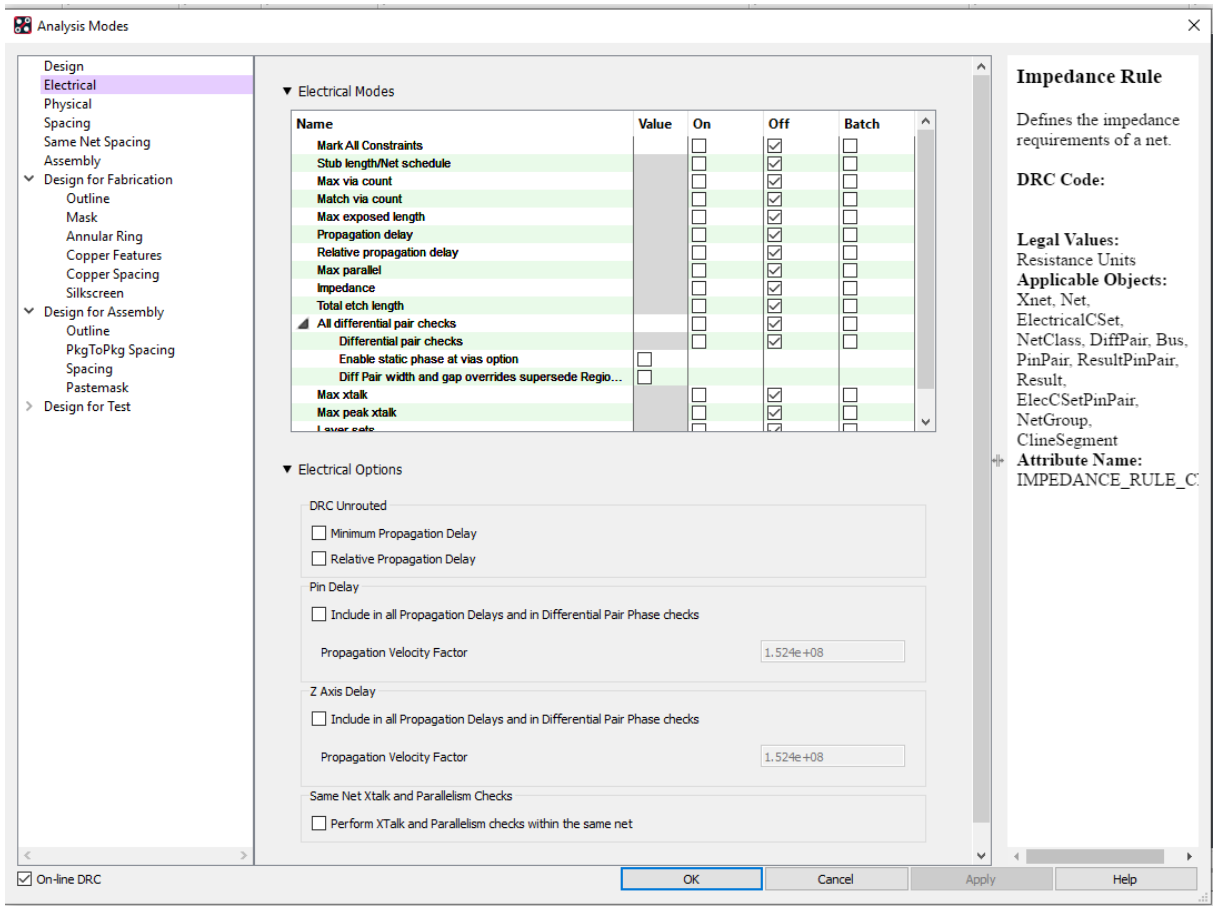
OrCAD PCB Designer Professional



Allegro PCB Designer



Allegro PCB Designer + High Speed Option



Stub length/Net schedule (OrCAD Professional and Allegro PCB Designer) – Specifies the maximum stub length in design units for daisy chain routing and enables the Verify schedule DRC.

Max via count (Allegro PCB Designer) – Specifies the maximum number of vias on the net.

Match via count (Allegro PCB Designer) – Specifies if vias should be matched in a group of nets.

Max exposed length (Allegro PCB Designer) – Specifies the maximum copper length in design units to be routed on outer layers.

Propagation delay (OrCAD Professional and Allegro PCB Designer) – The Propagation delay constraint is used to specify the minimum and maximum delay requirements for a Pin Pair. The constraint consists of three portions, which are defined as follows:

PROPAGATION_DELAY_PATH_TYPE defines which auto-generated PinPairs to check. It must be populated for all non-PinPair objects. PROPAGATION_DELAY_MIN Specifies the minimum allowable propagation delay, length or %length for the PinPairs. PROPAGATION_DELAY_MAX Specifies the maximum allowable propagation delay, length or %length for the PinPair(s).

Relative propagation delay (OrCAD Professional and Allegro PCB Designer) – The Relative Propagation Delay constraint is used to specify the matching or relative delay requirements for a group of PinPairs. To match implies that the PinPairs have the same delay within a specified tolerance. To be relative implies that the PinPairs have a delay which has some relation to a target in the group.

Max parallel (Allegro PCB Designer) – Specifies a matrix of length:distance constraints to control parallelism. The matrix can have up to four entries and defines the maximum length of two traces that can run parallel for a given gap/distance.

Impedance (OrCAD Professional and Allegro PCB Designer) – Specifies both the target and tolerance impedance requirement for etch. You specify the target impedance as an absolute value in Ohms. You can also specify the tolerance as an absolute value in Ohms or as a percentage.

Total etch length (OrCAD Professional and Allegro PCB Designer) – The Total Etch constraint is used to specify the minimum and maximum etch requirements for Xnet or Net.

All differential pair checks (All levels) – Enables all the DRC checks related to differential pairs.

Enable static phase at vias option - Optional behaviour will now perform the static phase length calculations from each differential pair via transition back to its designated Driver Pin and report a DRC marker when the constraint value is exceeded. Any via type transition, thru, BBVia, and micro will be checked as long as the differential pair members are transitioned from the same layer.

Differential Pair width and gap overrides supersede Region Constraint (Allegro PCB Designer) - Preserves the constraint resolution (precedence) of differential pair overrides. When enabled, differential pair overrides have a higher precedence than constraint regions. This property is automatically applied during uprev if any differential pair has any one of the following properties attached: DIFFP_PRIMARY_GAP, DIFFP_NECK_GAP, MIN_LINE_WIDTH, and MIN_NECK_WIDTH.

Note: You may not get the desired result if this option is enabled and differential pair Line and Gap constraints are applied by constraint region. The purpose of this property is to preserve the DRC status of an upreved design.

Enabling this option is not recommended for new designs. You should review your constraints and eliminate the need for this option.

Max xtalk (High Speed Option) – Specifies the maximum allowable crosstalk on the victim held at steady state high:low from all aggressor nets.

Max peak xtalk (High Speed Option) – Specifies the maximum allowable crosstalk on the victim held at steady state high:low from a single aggressor net.

Layer sets (OrCAD Professional and Allegro PCB Designer) - Specifies the list of acceptable layer sets. A single layer set is a collection of layer names upon which an object can be routed. If an object is routed on layers which are not contained in one set, a violation will be flagged. When the DRC runs, it also computes and ignores etch on outer layers which is necessary to fan-out for surface mount components. This ignored length is reported.

Return Path (High Speed Option) - Return Path DRC has been created to locate current return path issues based on selection criteria specified in Constraint Manager.

Electrical Options

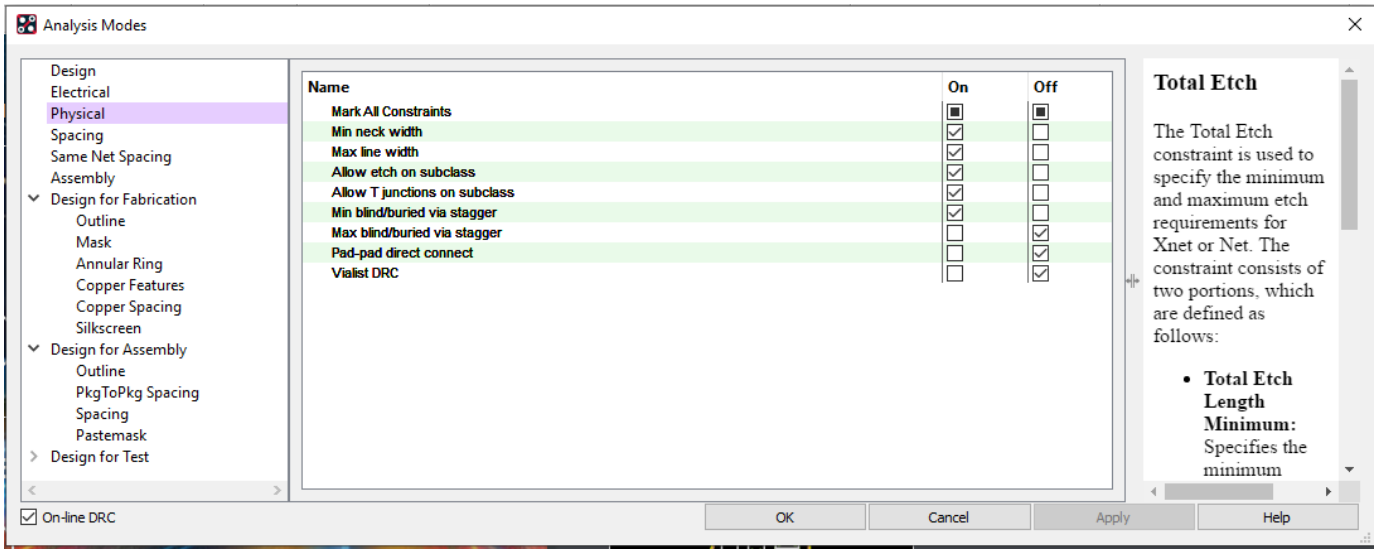
DRC Unrouted (OrCAD Professional and Allegro PCB Designer) – When checked--for either Minimum Propagation Delay or Relative Propagation Delay, Constraint Manager performs the rule check using the manhattan distances for ratsnest connections. This governs the respective DRC rule check, which you specify by clicking the DRC Modes tab.

Pin Delay (OrCAD Professional and Allegro PCB Designer) - When enabled, includes the delay associated with the interconnect that extends from a component pin to the die pad. This includes min/max/relative prop delays and differential pair phase tolerance constraint checks. You can access the Pin Delay column in the Relative Propagation Delay, Propagation Delay, or Differential Pair worksheets. The Pin Delay column has two fields (Pin1 and Pin2) that contain default values, which are derived from a component library or a board database. You can override the defaults by entering your own values. You enter constraints in worksheet cells using a unit of either time or length. You can enter a value in the Propagation Velocity Factor field to convert Pin Delay values to match the units entered in the worksheet cells. When you hover the mouse over an Actual cell, the status line indicates whether pin delay is included in the result.

Z-Axis Delay (OrCAD Professional and Allegro PCB Designer) - When enabled, includes the delay associated with a via that extends between connecting signal layers. Constraint Manager derives the Z axis delay length from the board thickness. When enabled, Constraint Manager includes via delay in length columns displayed in the Relative Propagation Delay, Propagation Delay, or Differential Pair worksheets. Z Axis Delay calculations use a unit of either time or length. If a constraint that uses Z Axis Delay is given in delay units, the Propagation Velocity Factor converts the actual length of the Z Axis Delay to the appropriate delay units. When you hover the mouse over an Actual cell, the status line indicates whether via delay is included in the result.

Same Net XTalk and Parallelism Checks (High Speed Option) - When enabled, performs DRC calculations for crosstalk and parallelism on themselves. When disabled, crosstalk and parallelism checks are made only between one net to every other net.

Physical



Min neck width - The minimum line width of a cline segment when in neck mode.

Max line width - The maximum width for the cline segments.

Allow etch on subclass – Specifies whether clines and shapes are allowed on this etch subclass**.**

Allow T junctions on subclass – Specifies whether T-junctions of cline segments are allowed and where they may form.

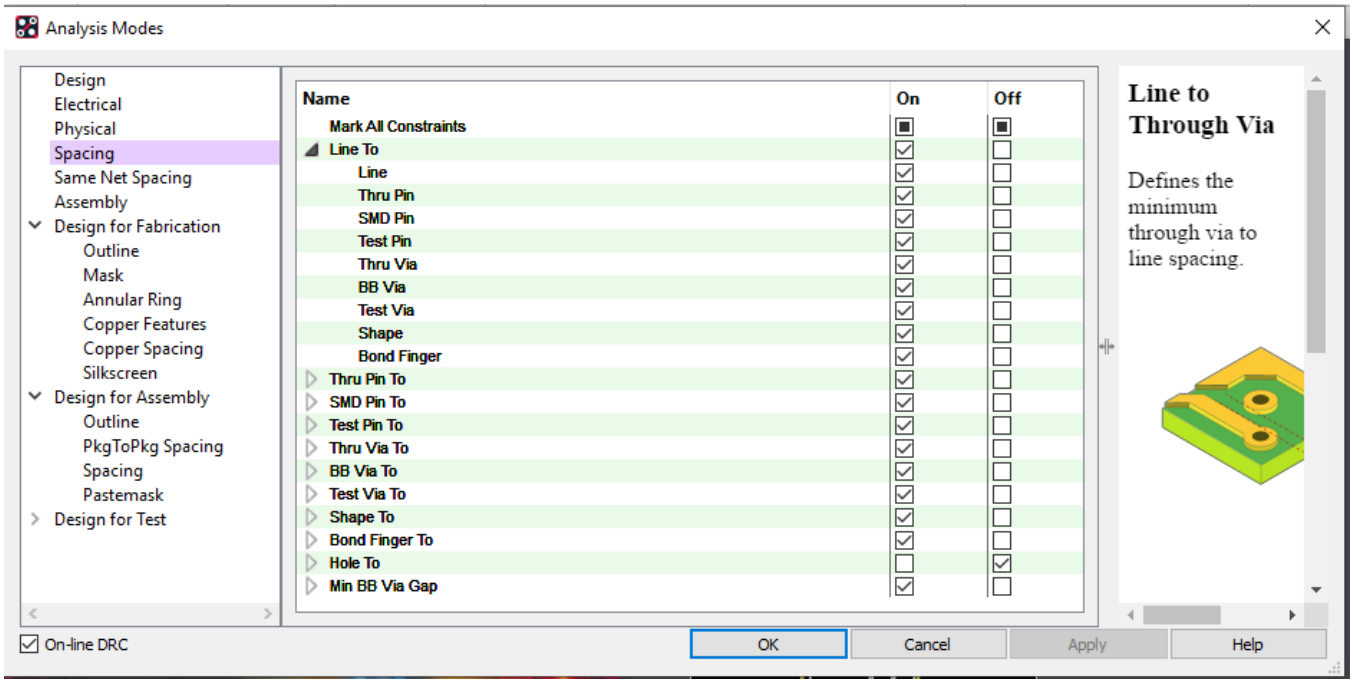
Min blind/buried via stagger – Specifies the minimum centre-to-centre distance between the connect point of one pin or via (the x,y location of the pin or via) and the connect point of the other, where the two pins or vias are on the same net and have a single connect line joining them.

Max blind/buried via stagger – Specifies the maximum centre-to-centre distance between the connect point of one pin or blind/buried via (the pin or via's x, y location) and the connect point of the other, where the two pins or vias are on the same net and have a single connect line joining them.

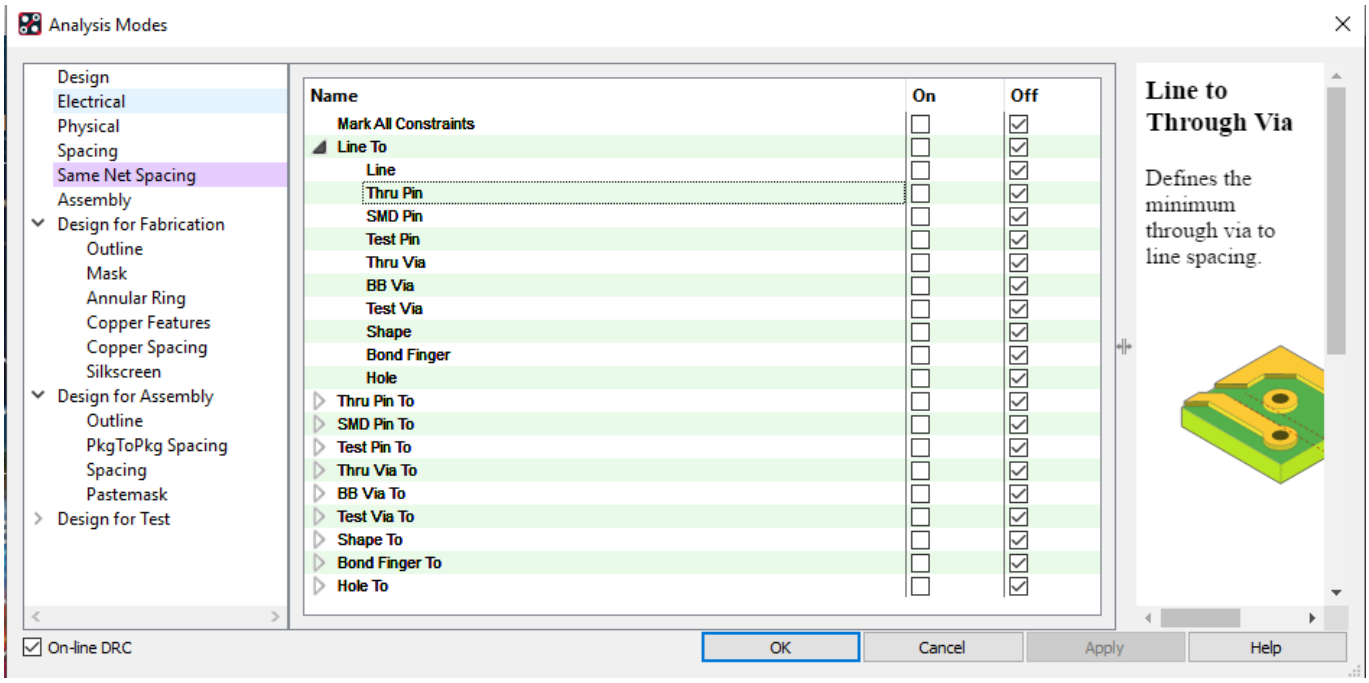
Pad-pad direct connect – Specifies whether a pin/via whose connect point lies within the extents of another pin/via forms a direct connection without the presence of an intermediate cline.

Vialist DRC - Lists the padstacks in the database of the current design which are allowed for routing. These are controlled by the Physical Constraint Set.

Spacing

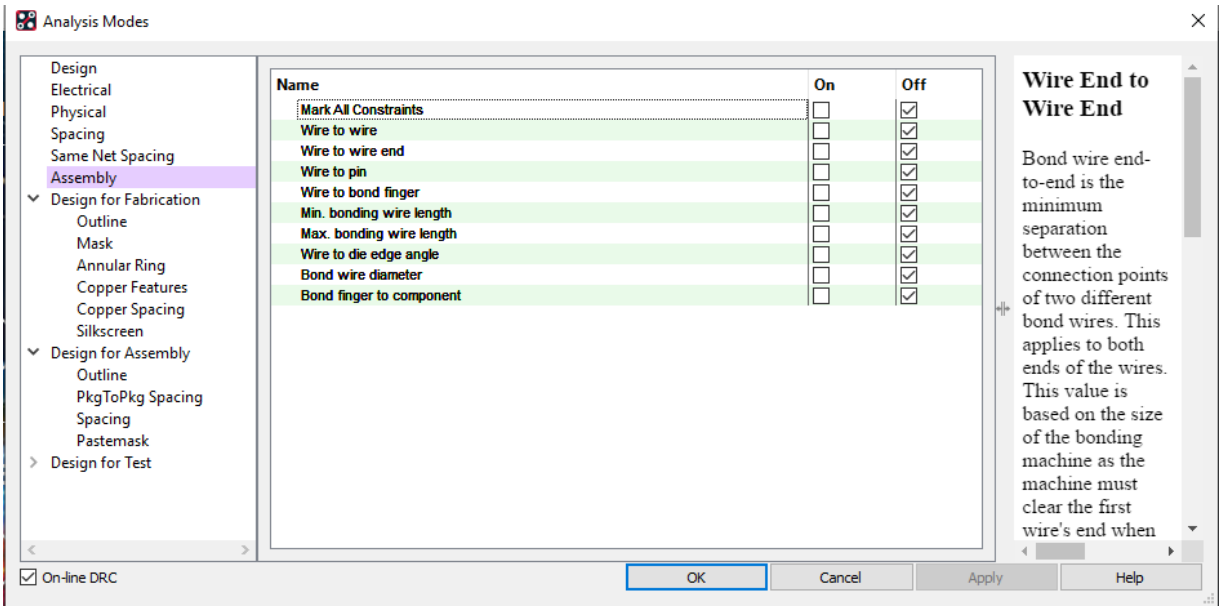


Same Net Spacing



The Spacing and same net spacing DRC modes covers all the relevant spacing checks. These are all self-explanatory based on the name for example Line to Line would enable the Line to Line check allowing users to see a DRC if the minimum Line to Line value was not met. If you need a detailed description of these checks please refer to constraintcore.pdf as mentioned at the beginning of this note.

Assembly



Wire to wire (Allegro PCB Designer) – This rule applies to the space between two bond wires that are on the same side of the package substrate. Wires which share an end point object, such as a die-to-die bond wire connecting to the same pin as a die-to-substrate bond wire, are not checked. The distance is measured as the minimum 2D separation between the two wires.

Wire to wire end (Allegro PCB Designer) – Bond wire end-to-end is the minimum separation between the connection points of two different bond wires. This applies to both ends of the wires. This value is based on the size of the bonding machine as the machine must clear the first wire's end when placing the second wire.

Wire to pin (Allegro PCB Designer) – This rule applies only to the space between a bond wire and die pad. The die pad to which the wire connects is excluded from the check. The distance is measured as the minimum 2D separation between the wire and die pad edge, ignoring any possible height difference between the wire and pad.

Wire to bond finger (Allegro PCB Designer) – This rule applies only to the space between a bond wire and finger, and does not apply to die-to-die bond wires. The distance is measured as the minimum 2D separation between the wire and finger's conductor pad edge, ignoring any finger pads on BONDING WIRE, DIELECTRIC, or SOLDERMASK layers.

Min bonding wire length (Allegro PCB Designer) – This rule applies to the minimum length of every die pad-to-substrate finger bond wire connection in the design. Die-to-die bond wires are handled by a separate rule. Length is measured as the 2D distance between the start and end point of the wire.

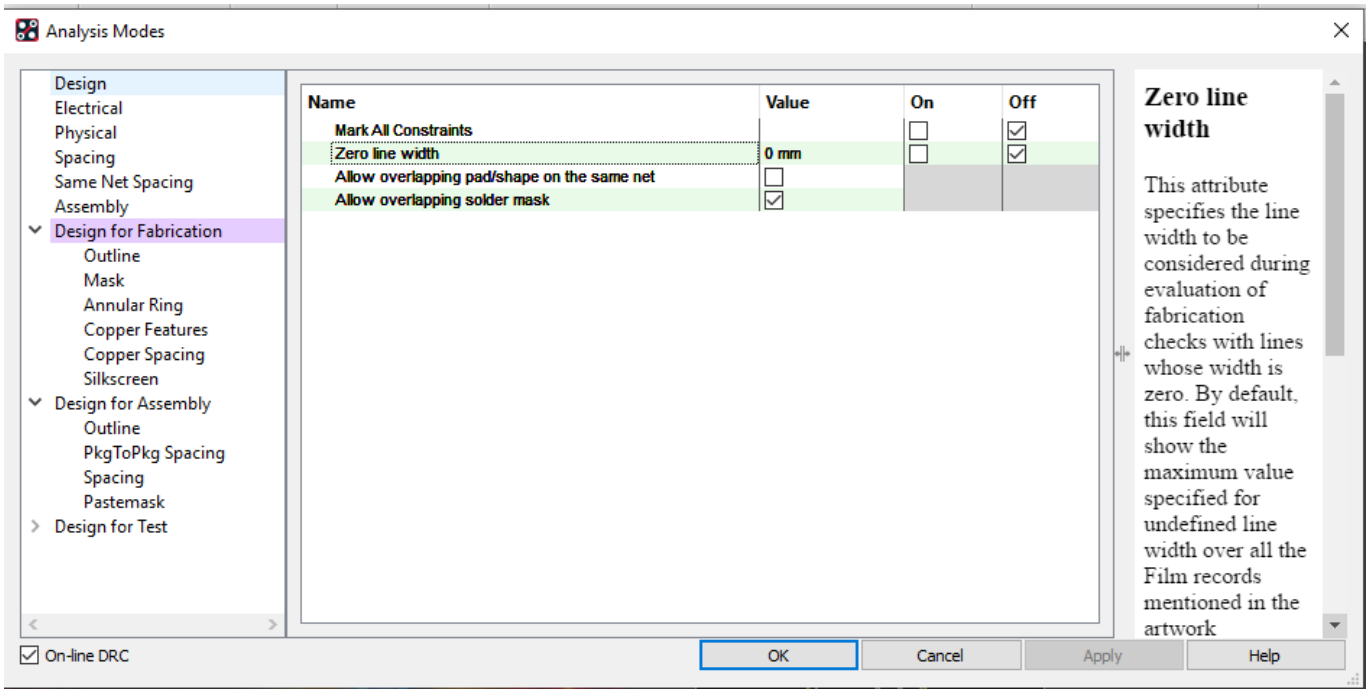
Max bonding wire length (Allegro PCB Designer) – This rule applies to the maximum length of every die pad-to-substrate finger bond wire connection in the design. Die-to-die bond wires are handled by a separate rule. Length is measured as the 2D distance between the start and end point of the wire.

Wire to die edge angle (Allegro PCB Designer) – This rule applies to the angle of every bond wire in the design, regardless of the start and end connection types. Wire maximum angle refers to the maximum angle at which a wire may be placed. The tool measures this angle relative to the side of the die that the wire crosses.

Bond wire diameter (Allegro PCB Designer) – Specifies the required diameter to use when bonding the die into the package. Use this value when calculating clearance values for bond finger-to-wire and bond wire-to-wire spacing checks.

Bond finger to component (Allegro PCB Designer) – Bond finger component edge spacing is the minimum separation required between a bond finger and the edge of a component (typically die or discrete) on the same edge of the package substrate. Typically, this is the clearance required to ensure that the capillary clears the component edge when adding the wires.

Design for Fabrication

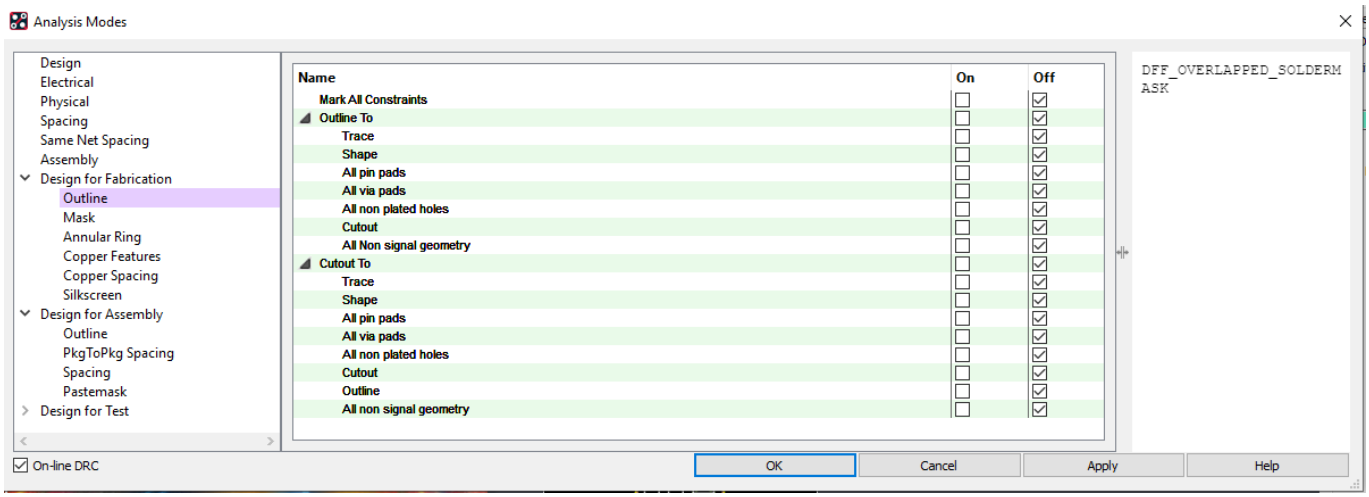


Zero line width - This attribute specifies the line width to be considered during evaluation of fabrication checks with lines whose width is zero. By default, this field will show the maximum value specified for undefined line width over all the Film records mentioned in the artwork parameter record. Set new values to override the artwork parameter value for evaluation of fabrication checks. This value is also applicable for text line if photo plot width is zero. For texts, the DRC engine looks for photo plot width specified in the text block and if that is zero, this value will be assumed.

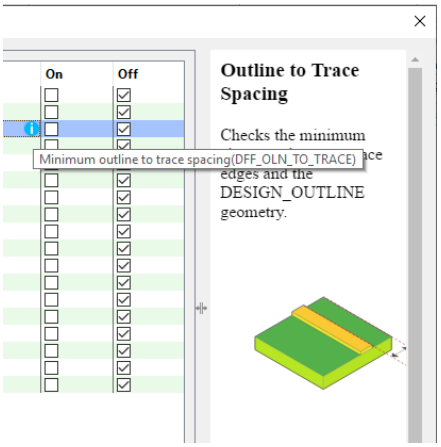
Allow overlapping pad/shape on the same net - This is an option to specify that overlapping pad with shape or pad with pad should not be treated as violation in case they are on the same net. The pads can be from via or pin. In copper spacing checks, if two pads of the same net overlap, or if a pad overlaps with a shape on the same net in case of static shape, fabrication DRC violations are reported with actual value as OVERLAP. This may be perfectly valid case from manufacturing perspective. If this option is set, those DRCs will not be reported.

Allow overlapping soldermask – As above but for soldermask defined pads.

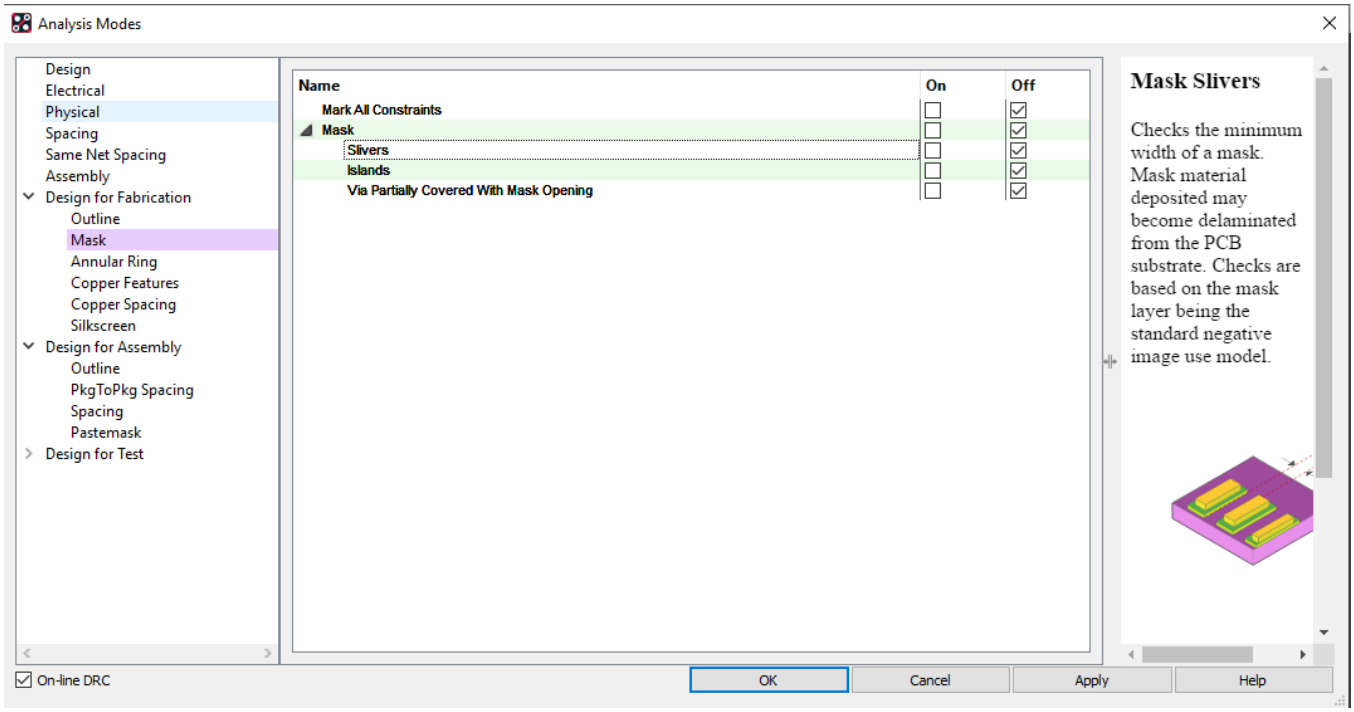
Design for Fabrication - Outline



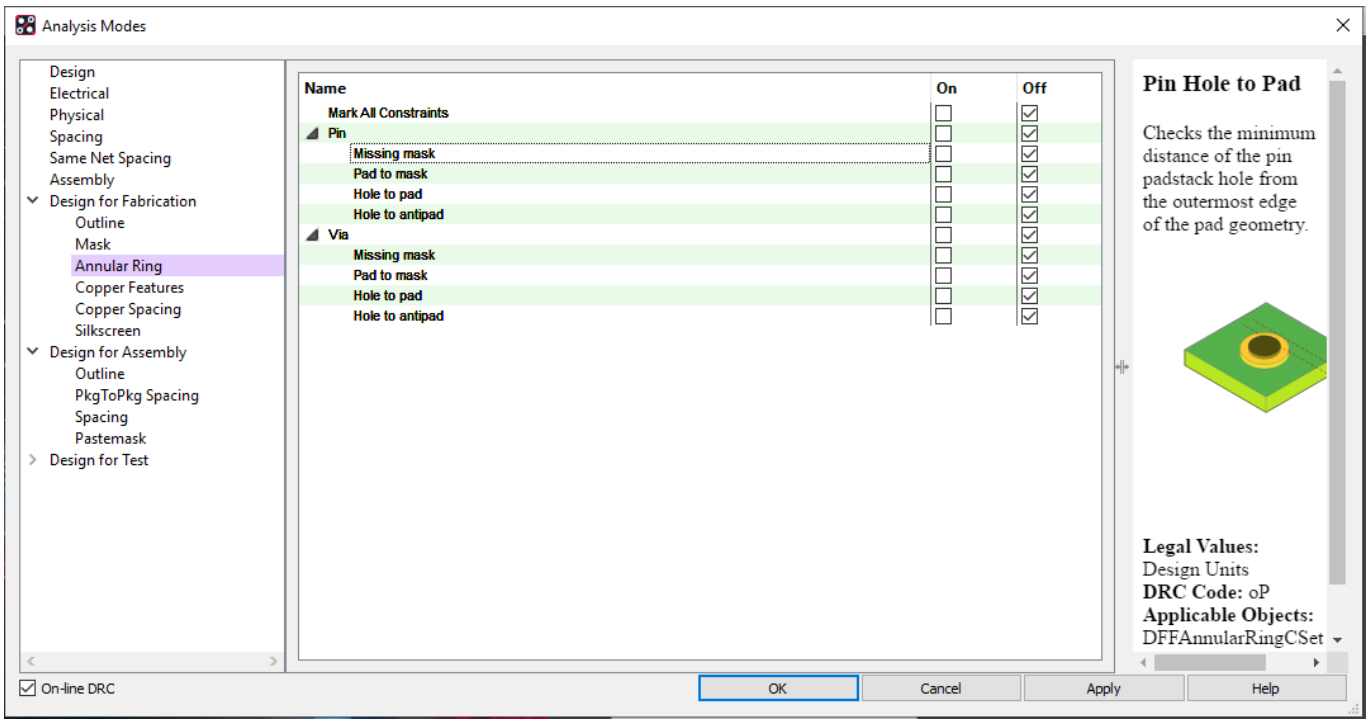
Design_Outline and Cutout to objects check the relevant objects, if you hover over each rule Outline to Trace (Info button) then a graphical description of the DRC rule is shown. Available for most DRC modes.



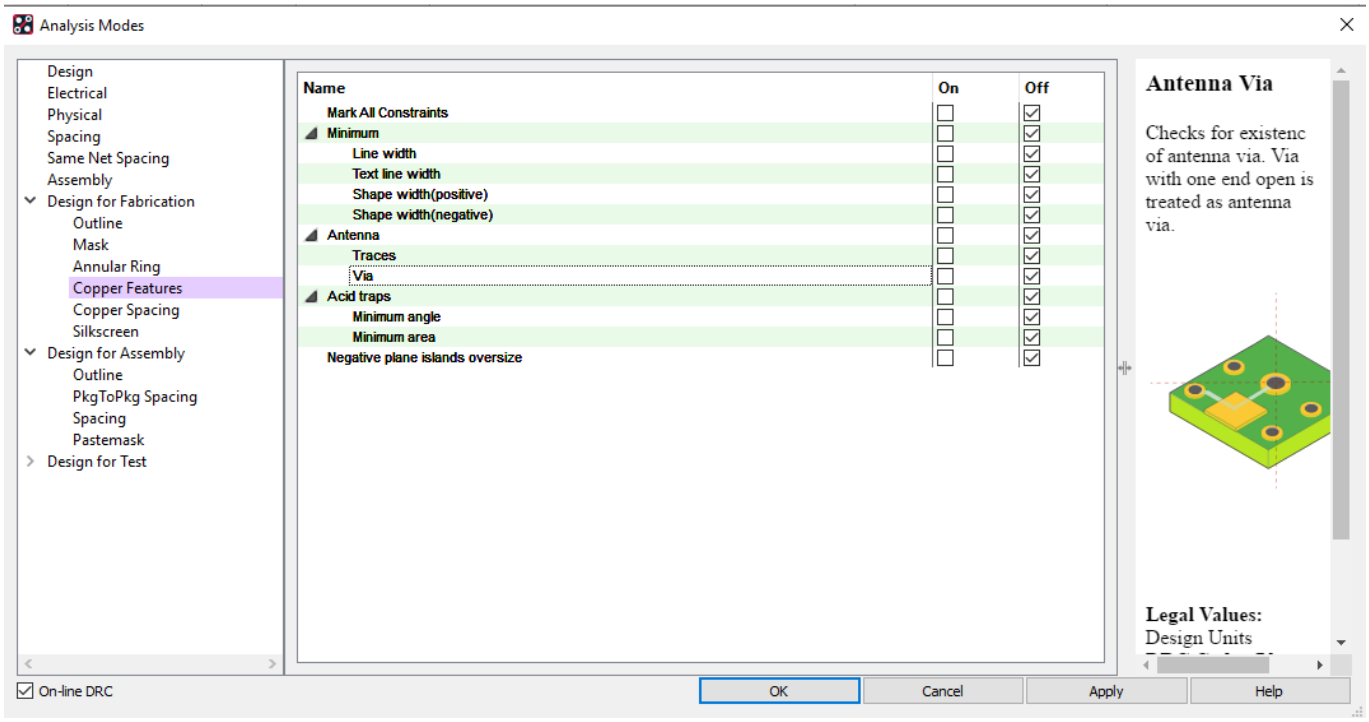
Design for Fabrication – Mask



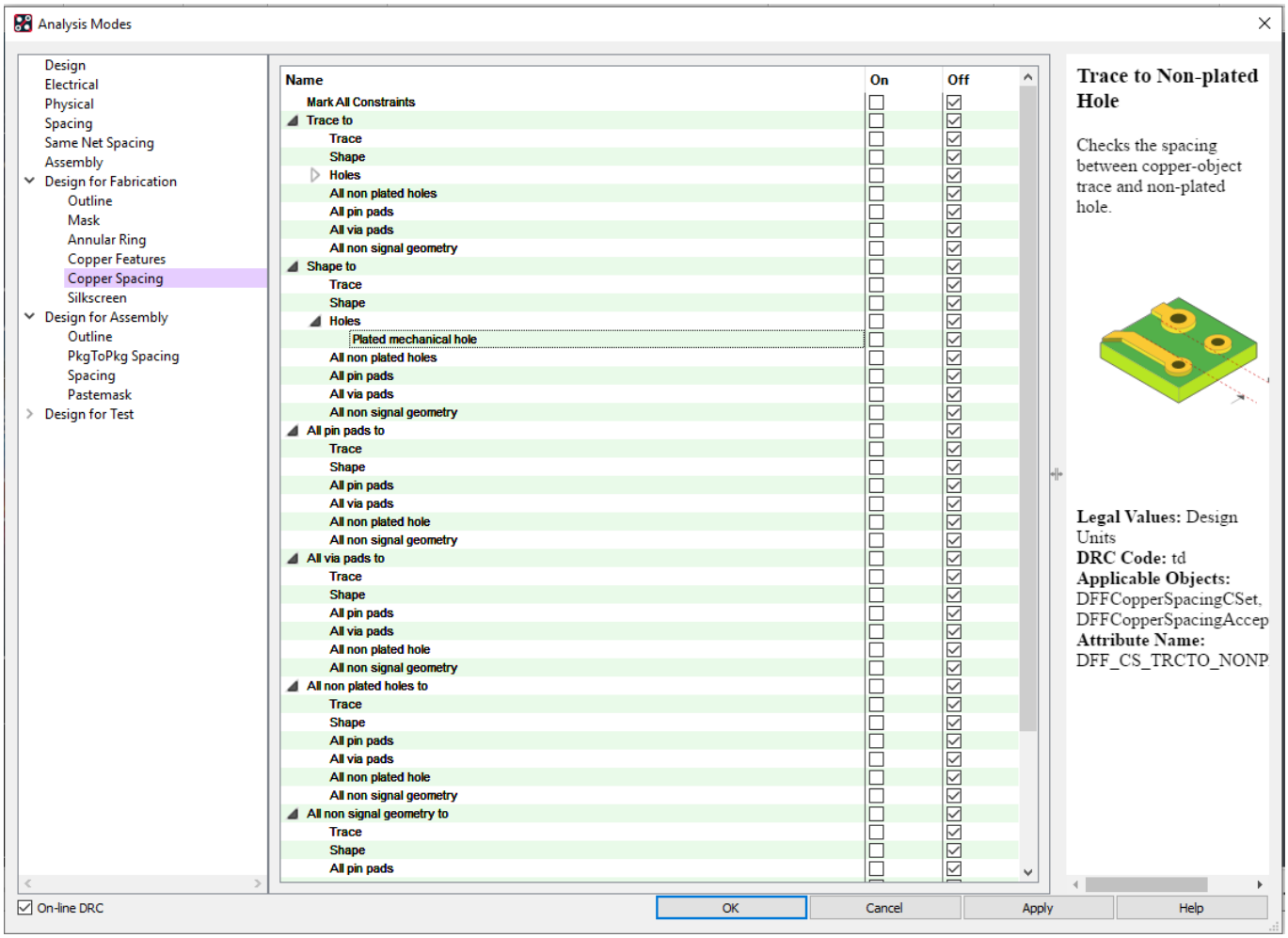
Design for Fabrication – Annular Ring



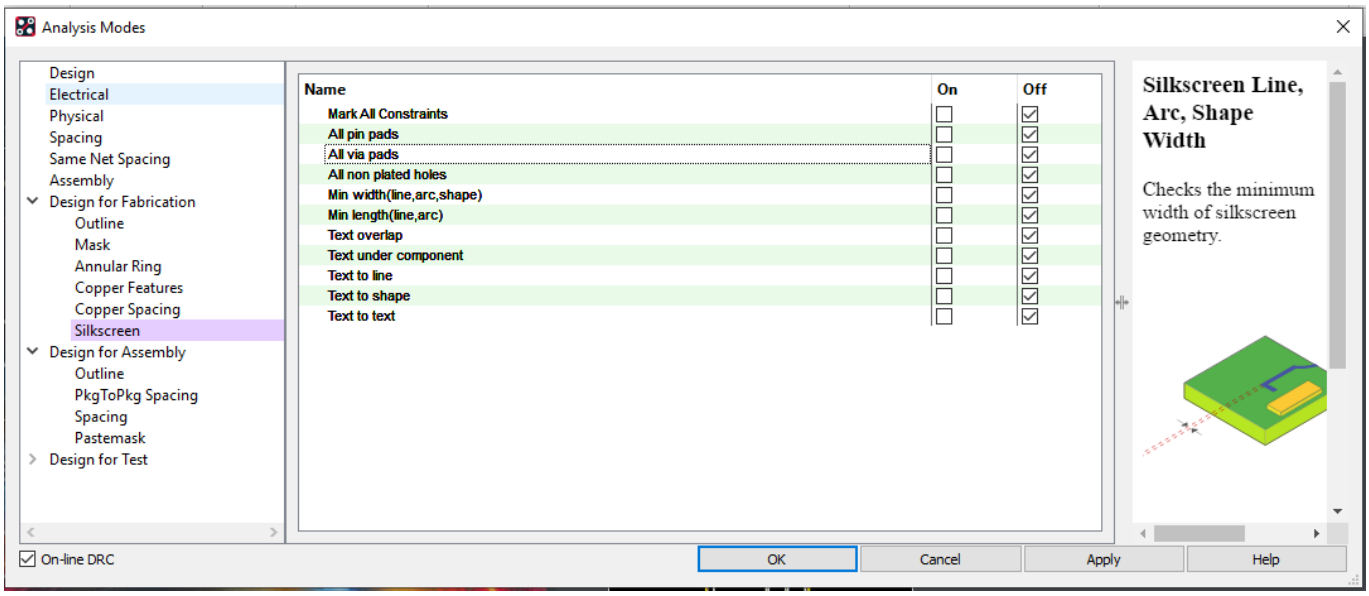
Design for Fabrication – Copper Features



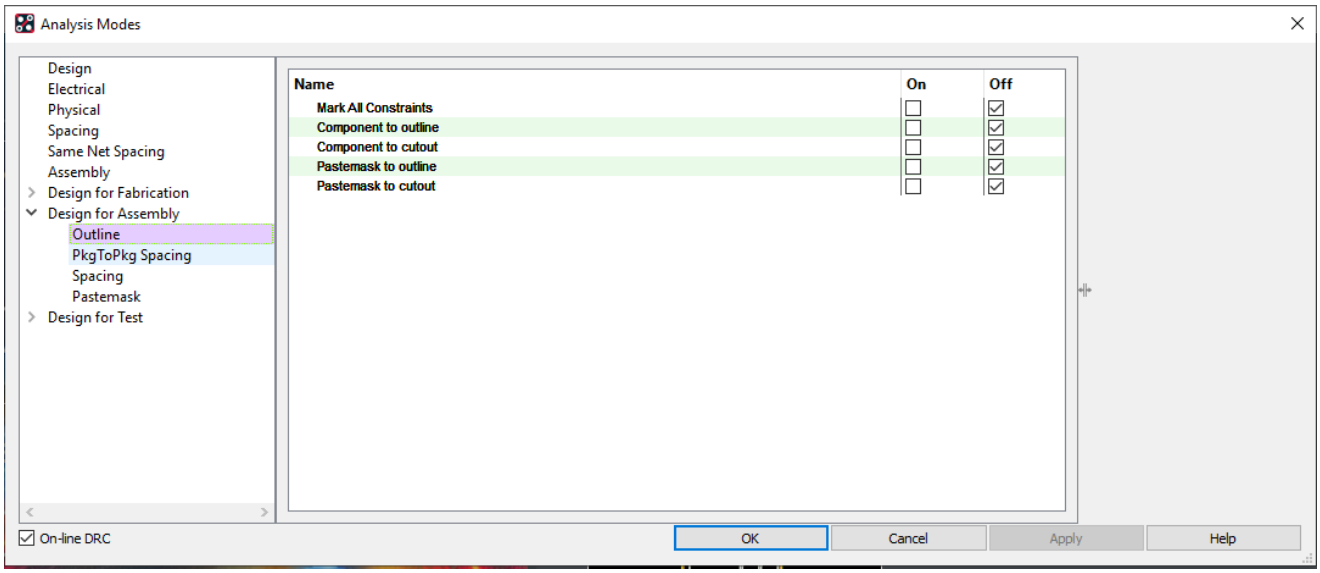
Design for Fabrication – Copper Spacing



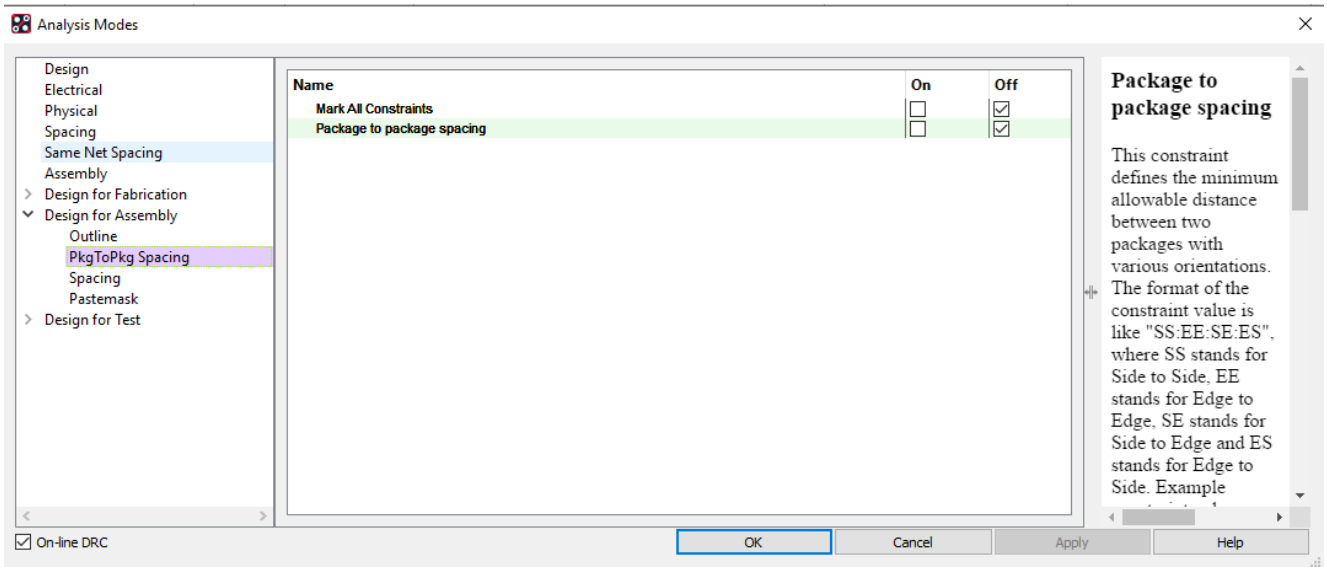
Design for Fabrication – Silkscreen



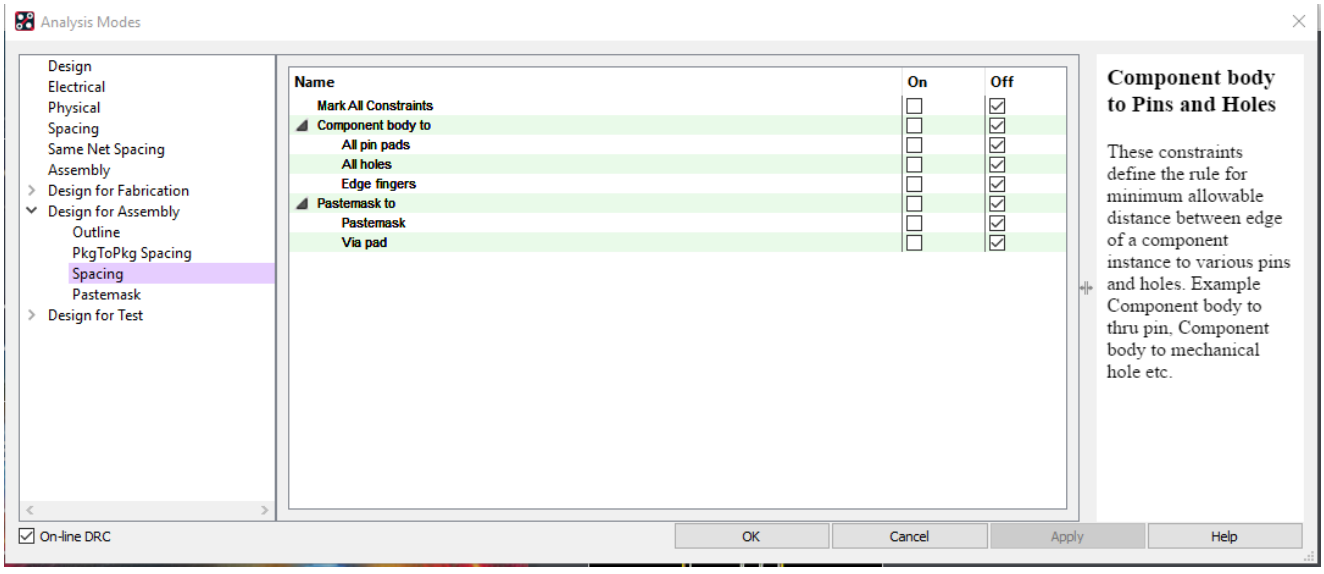
Design for Assembly – Outline



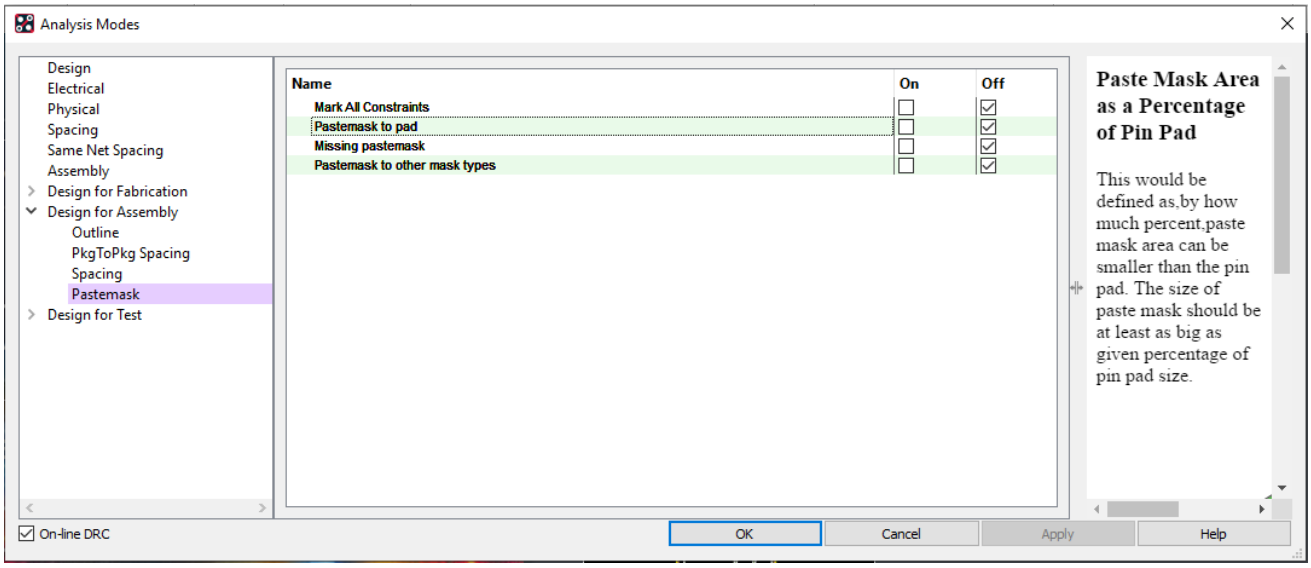
Design for Assembly – PkgToPkg Spacing



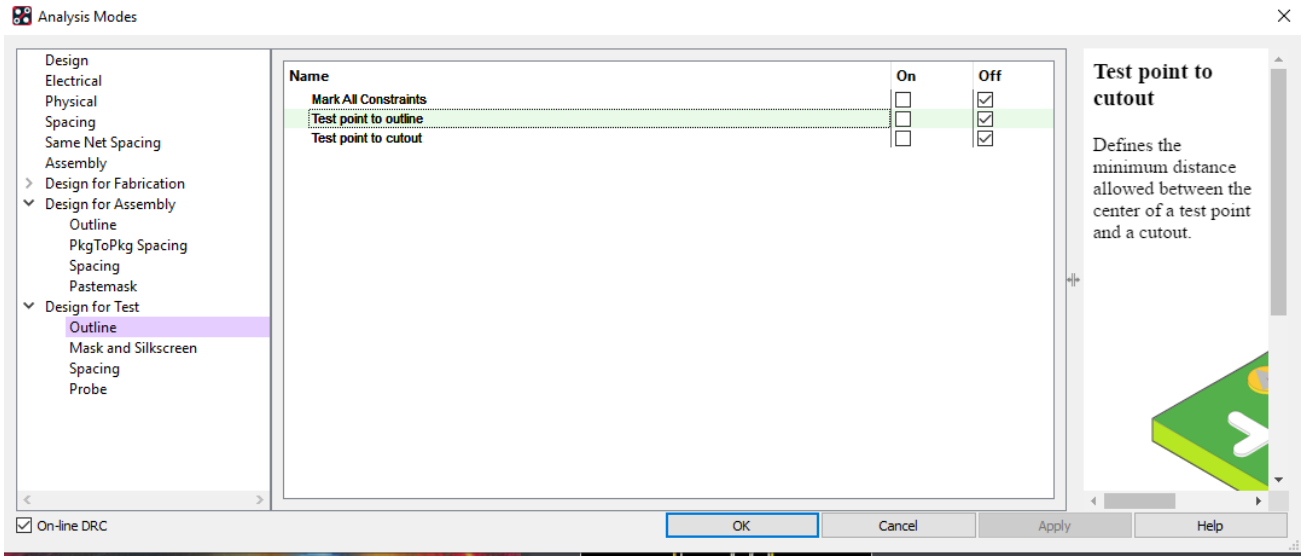
Design for Assembly – Spacing



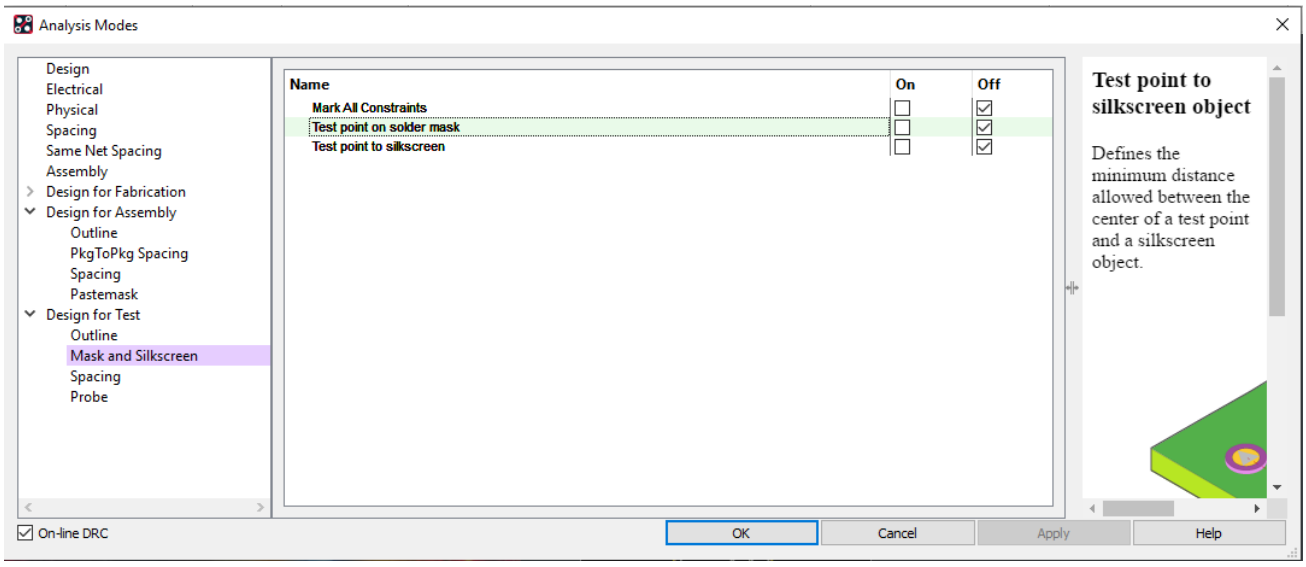
Design for Assembly - Pastemask



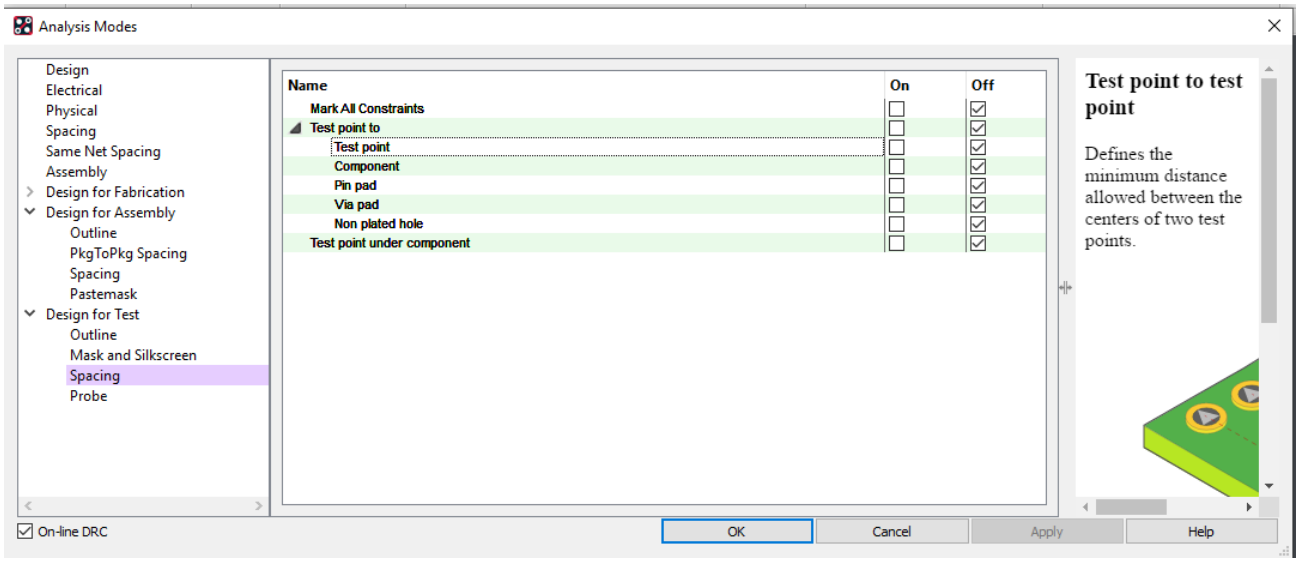
Design for Test – Outline



Design for Test – Mask and Silkscreen



Design for Test – Spacing



Design for Test - Probe