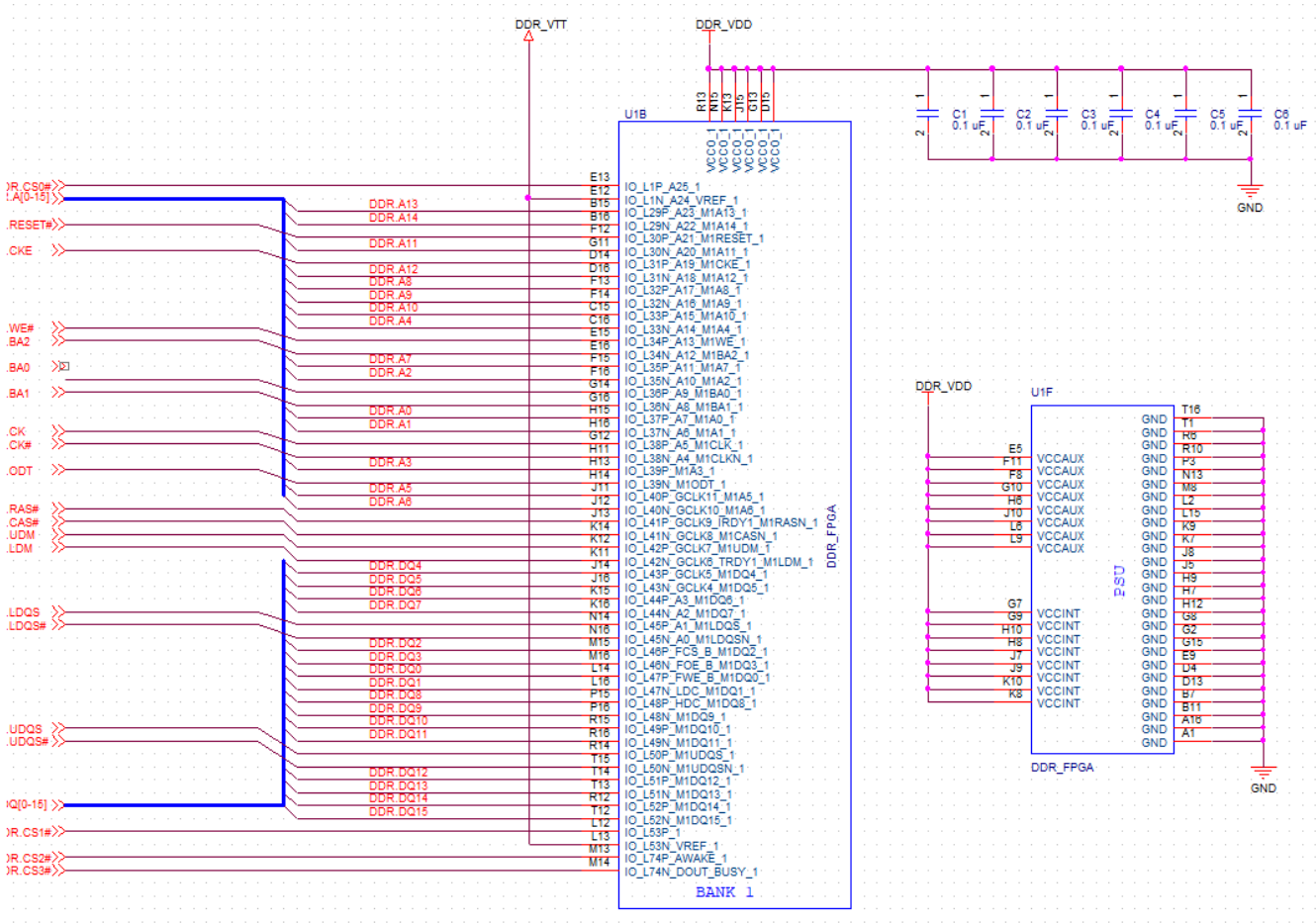
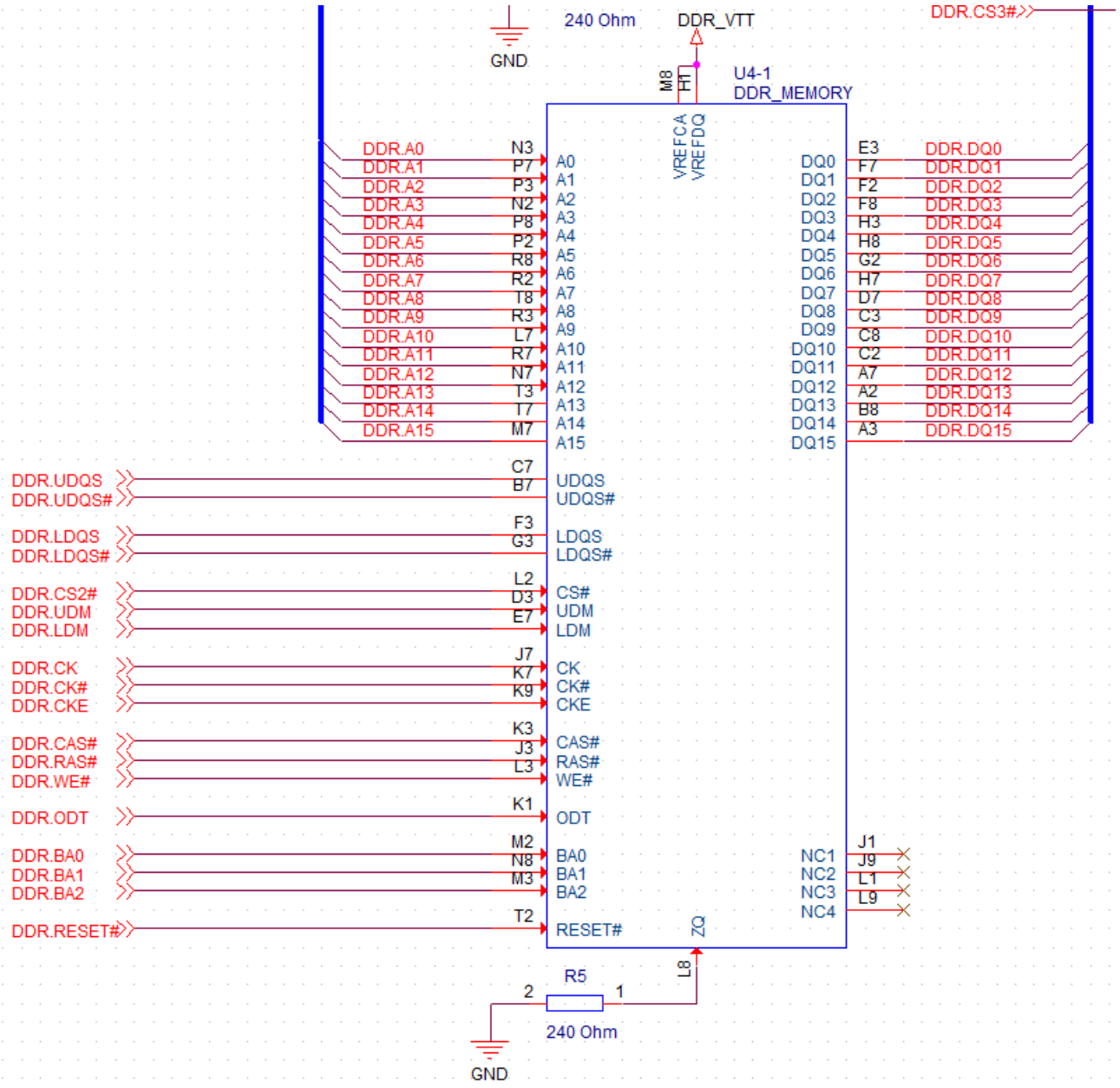
DDR Constraints example

This application note will describe the basic setup options required to constraint a DDR memory. This is a generic example of how to set and define constraints using Cadence OrCAD PCB Professional and should be checked with your own specific design guidelines / rules from the component manufacturers. This is not a working or tested version of DDR memory but an example of how to set Constraints using the Cadence PCB tools. The version used in this example is 17.4-2019 S003, although the methods used should be consistent with other versions of this software provided that they enable access to the relevant Electrical worksheets in Constraint Manager. There are also different methods available to achieve this setup, for example by using Allegro PCB Designer + High Speed Option which would simplify the pin pair creation and by using SI Explorer, which would provide the ability to make templates of the nets in question, then apply those templates to netclasses to achieve the same results more quickly.

DDR Schematic

Click here for a link to the PDF file for a simple schematic used in this example. It contains one FPGA and four memory devices plus decoupling capacitors and termination resistors. The general idea for this setup is to route these together using a daisy chain (fly-by) topology meaning start the routing from the controller to the first memory device then the next and so on. Based on this schematic U1 > U2 > U3 > U4 > U5, The following two pictures show the FPGA device and one of the memory devices. Open the PDF for a full view of the schematic.





Constraints

All the rules defined are setup using Constraint Manager. This can be accessed from either OrCAD Capture or PCB Editor. Both methods allow access to a full Constraint Manager. If setting constraints via the front end (OrCAD Capture) the key is to ensure that the schematic and PCB stay in sync. **ALWAYS** ensure using the Design Sync command from the board file into the schematic has been completed before making changes.

Physical and Spacing Constraints

This design has three physical rules and one spacing rule. (You may also need additional physical and spacing rules depending on your specific design). Constraint Regions (rules by area) may also be required, for example where additional rules may be required to neck down the track and decrease gap rules to allow you to route the board. The three physical rules are as shown below and can be created by selecting the default rule and right click > Create > Physical CSet, then enter the required name and setting the appropriate values.

DDR_EXAMPLE	DEFAULT	0.1500	0.0000	0.1000	5.0000	0.0000	0.0000	0.0000	0.0000	0.0000	VIA-0_45-0_2
DEFAULT		0.1500	0.0000	0.1000	5.0000	0.0000	0.0000	0.0000	0.0000	0.0000	VIA-0_45-0_2
DIFFPAIR		0.1500	0.0000	0.1000	10.0000	0.1000	0.1500	0.0000	0.0500	0.0500	VIA-0_45-0_2
POWER		0.5000	0.0000	0.1400	5.0000	0.0000	0.0000	0.0000	0.0000	0.0000	VIA-0_45-0_2

For spacing rules, the default rule is good enough for this example with all values set to 0.15mm.

Objects		Line To	Thru Pin To	SMD Pin To	Test Pin To	Thru Via To	BB Via To	Test Via To	Shape To	Bond Finger To	Hole To
Name	Referenced Spacing CSet	All	All	All	All	All	All	All	All	All	All
		mm	mm	mm	mm	mm	mm	mm	mm	mm	mm
*	*	*	*	*	*	*	*	*	*	*	*
DDR_EXAMPLE	DEFAULT	0.1500	0.1500	0.1500	0.1500	0.1500	0.1500	0.1500	0.1500	0.1500	0.1500
DEFAULT		0.1500	0.1500	0.1500	0.1500	0.1500	0.1500	0.1500	0.1500	0.1500	0.1500

The Power rule is applied to the three power nets DDR_VDD, DDR_VTT and GND and the DIFFPAIR rules are applied to three differential pairs DP_LDQS, DP_CK and DP_UDQS. These were made with Objects>Create>Differential Pair and the relevant net names selected and named. These have been grouped into a Netclass to simplify the constraints.

NCIs		DIFFPAIRS(3)	DIFFPAIR
DPr		DP_CK	DIFFPAIR
Net		DDR.CK	DIFFPAIR
Net		DDR.CK#	DIFFPAIR
DPr		DP_LDQS	DIFFPAIR
Net		DDR.LDQS	DIFFPAIR
Net		DDR.LDQS#	DIFFPAIR
DPr		DP_UDQS	DIFFPAIR
Net		DDR.UDQS	DIFFPAIR
Net		DDR.UDQS#	DIFFPAIR
NCIs		POWER(3)	POWER
Net		DDR_VDD	POWER
Net		DDR_VTT	POWER
Net		GND	POWER

Electrical Constraints

We will start by creating some netclasses to define the nets into their relevant groups. In Constraint Manager>Electrical>Net>Routing>Wiring group select DDR.A0>DDR.A15 then right click>Create>Netclass and name this ADDRESS. We also need to make two byte lanes that consist of DDR.DQ0-7, DDR.LDM and DDR.LDQS# in one and DDR.DQ8-15, DDR.UDM and DDR/UDQS# in the other. These have been named BYTELANE0 and BYTELANE1. You will notice that only one half of each differential pair has been put into each bytelane. This will allow the diff pair members to be matched with one set of constraints (static phase) and avoid over constraining the design.

NCIs		ADDRESS(16)
Net		DDR.A0
Net		DDR.A1
Net		DDR.A2
Net		DDR.A3
Net		DDR.A4
Net		DDR.A5
Net		DDR.A6
Net		DDR.A7
Net		DDR.A8
Net		DDR.A9
Net		DDR.A10
Net		DDR.A11
Net		DDR.A12
Net		DDR.A13
Net		DDR.A14
Net		DDR.A15

NCIs		BYTELANE0(10)
Net		DDR.DQ0
Net		DDR.DQ1
Net		DDR.DQ2
Net		DDR.DQ3
Net		DDR.DQ4
Net		DDR.DQ5
Net		DDR.DQ6
Net		DDR.DQ7
Net		DDR.LDM
Net		DDR.LDQS#

NCIs		BYTELANE1(10)
Net		DDR.DQ8
Net		DDR.DQ9
Net		DDR.DQ10
Net		DDR.DQ11
Net		DDR.DQ12
Net		DDR.DQ13
Net		DDR.DQ14
Net		DDR.DQ15
Net		DDR.UDM
Net		DDR.UDQS#

Create an Electrical CSet for the differential pairs so under Constraint Manager>Electrical>Electrical Constraint Set >Routing>Differential Pair make a new rule for the differential pairs, remember that we only need to define the uncoupled length, static and dynamic phase rules since the coupling parameters (track and gap) are covered by physical rules.

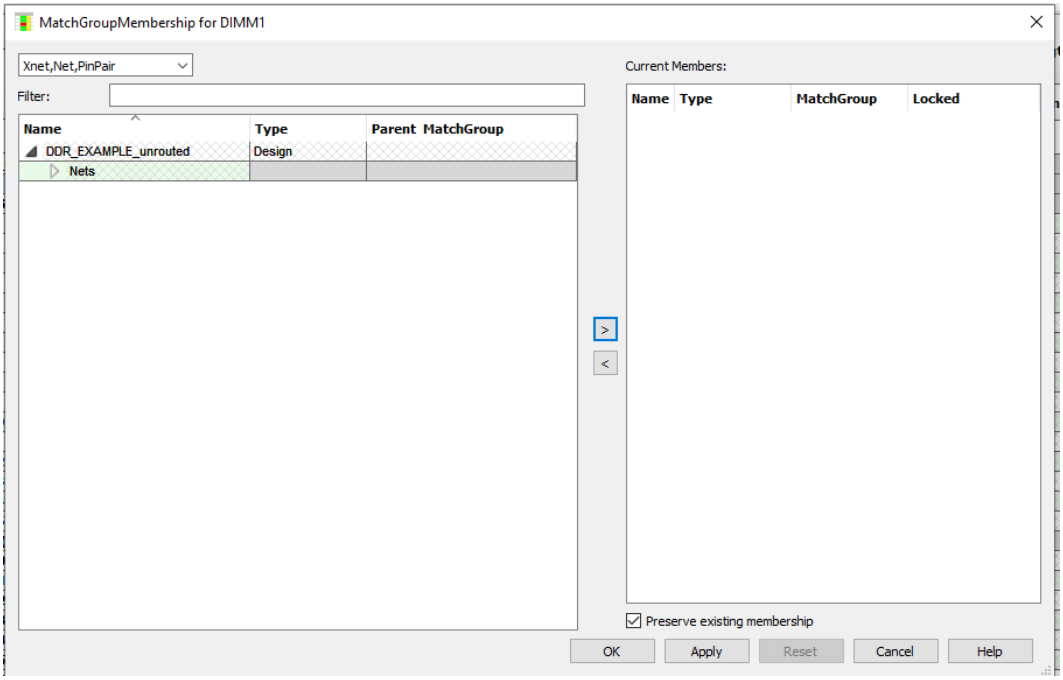
Objects			Uncoupled Length		Static Phase Tolerance	Dynamic Phase	
Type	S	Name	Gather Control	Max		Max Length	Tolerance
				mm	mm	mm	mm
*	*	*	*	*	*	*	*
Dsn		DDR_EXAMPLE					
ECS		DIFFPAIR	Ignore	5.0000	2 mm	10.0000	3 mm

Once the rule is created, apply this to the three differential pairs.

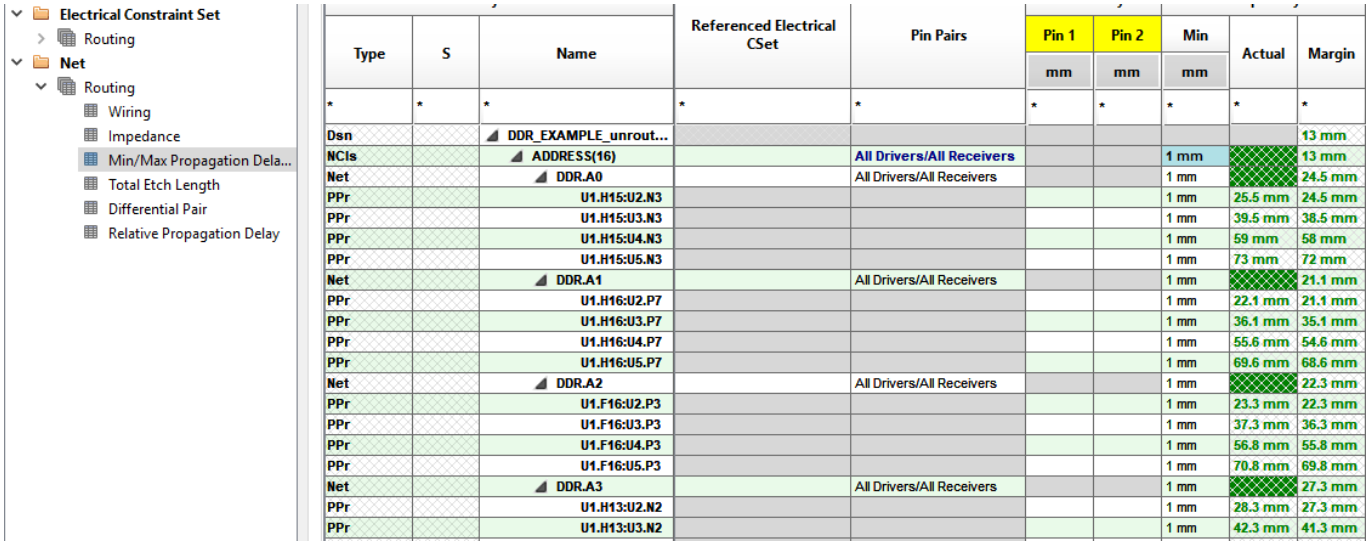
Matched Groups.

The IC rules typically define how and what nets are required to be length matched and by what tolerance. For the first part we need to match the Address and Control lines from the FPGA to the first memory device (U1>U2). Locate the relevant nets in Constraint Manager>Electrical>Net>Routing>Relative Propagation Delay worksheet and right click>Create>Pin Pair, choose the start and end and define the pin pairs required. (If you had access to an Allegro PCB Designer + High Speed license this could be achieved using Sig Explorer by making a topology template).

Another method would be to create a Match Group name (say DIMM1) then select the Match Group name and choose right click>Match Group Members, you will notice that this only lists Nets.

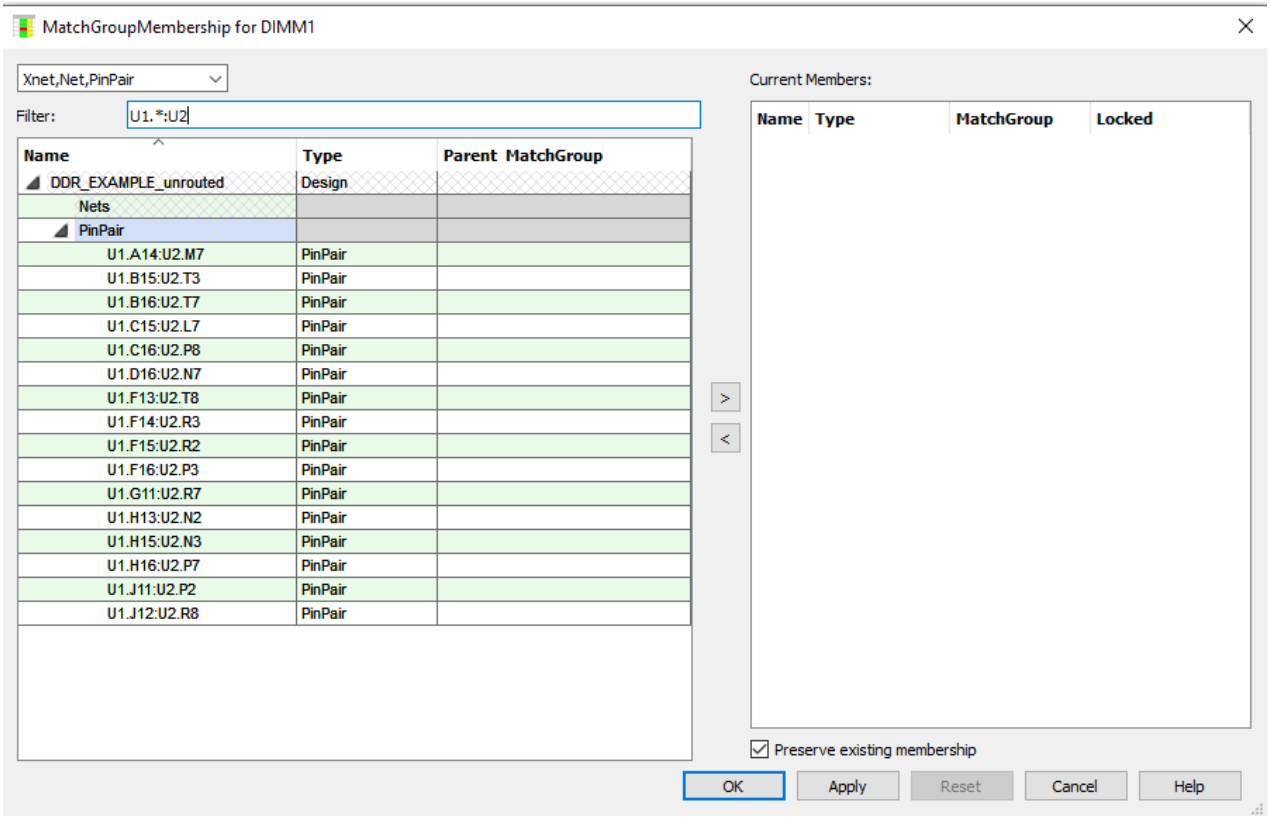


To generate the PinPairs quickly open the Min/Max Propagation Delay worksheet and specify a value for Min length for the Address and Bytelane classes (1mm will do) and OrCAD Professional automatically generates all the relevant pin pairs.



Type	S	Name	Referenced Electrical CSet	Pin Pairs	Pin 1 mm	Pin 2 mm	Min mm	Actual	Margin
*	*	*	*	*	*	*	*	*	*
Dsn		DDR_EXAMPLE_unrout...							13 mm
NCls		ADDRESS(16)		All Drivers/All Receivers			1 mm		13 mm
Net		DDR.A0		All Drivers/All Receivers			1 mm		24.5 mm
PPr		U1.H15:U2.N3					1 mm	25.5 mm	24.5 mm
PPr		U1.H15:U3.N3					1 mm	39.5 mm	38.5 mm
PPr		U1.H15:U4.N3					1 mm	59 mm	58 mm
PPr		U1.H15:U5.N3					1 mm	73 mm	72 mm
Net		DDR.A1		All Drivers/All Receivers			1 mm		21.1 mm
PPr		U1.H16:U2.P7					1 mm	22.1 mm	21.1 mm
PPr		U1.H16:U3.P7					1 mm	36.1 mm	35.1 mm
PPr		U1.H16:U4.P7					1 mm	55.6 mm	54.6 mm
PPr		U1.H16:U5.P7					1 mm	69.6 mm	68.6 mm
Net		DDR.A2		All Drivers/All Receivers			1 mm		22.3 mm
PPr		U1.F16:U2.P3					1 mm	23.3 mm	22.3 mm
PPr		U1.F16:U3.P3					1 mm	37.3 mm	36.3 mm
PPr		U1.F16:U4.P3					1 mm	56.8 mm	55.8 mm
PPr		U1.F16:U5.P3					1 mm	70.8 mm	69.8 mm
Net		DDR.A3		All Drivers/All Receivers			1 mm		27.3 mm
PPr		U1.H13:U2.N2					1 mm	28.3 mm	27.3 mm
PPr		U1.H13:U3.N2					1 mm	42.3 mm	41.3 mm

Return to the Relative Propagation delay worksheet, select the Match Group name and right click>Match Group Members and now notice that the Pin Pairs are available to be selected. Use the Filters for U1.*:U2 to filter the list and move the objects to cerate the match group members. Repeat for the remainder of the match groups you require.



Remember to remove the Min Propagation delay rule you defined to aid in the quick generation of Pin Pairs.

Once all the pin pairs are created, select them all (left click + shift left click) then right click>Create>Match Group. Specify the name. Once created set the Delta:Tolerance values and either accept a default Target (longest unrouted member) or choose your required target.

To visualise this, enable Analysis>Analysis Mode>Electrical and turn on DRC unrouted Relative Propagation Delay, or right click the Delta:Tolerance cell of the pin pair you want to be the Target value and choose Set as Target.

MGrp		DDR_ADDR_CNTRL_DIMM1(25)		All Drivers/All Receivers			Global	0 mm:1 mm		10 mm
PPr		U1.H15:U2.N3 [DDR.A0]					Global	0 mm:1 mm	4.4 mm	3.4 mm
PPr		U1.H16:U2.P7 [DDR.A1]					Global	0 mm:1 mm	1 mm	0 mm
PPr		U1.F16:U2.P3 [DDR.A2]					Global	0 mm:1 mm	2.2 mm	1.2 mm
PPr		U1.H13:U2.N2 [DDR.A3]					Global	0 mm:1 mm	7.2 mm	6.2 mm
PPr		U1.C16:U2.P8 [DDR.A4]					Global	0 mm:1 mm	4.8 mm	3.8 mm
PPr		U1.J11:U2.P2 [DDR.A5]					Global	0 mm:1 mm	11 mm	10 mm
PPr		U1.J12:U2.R8 [DDR.A6]					Global	0 mm:1 mm	6 mm	5 mm
PPr		U1.F15:U2.R2 [DDR.A7]					Global	0 mm:1 mm	4.8 mm	3.8 mm
PPr		U1.F13:U2.T8 [DDR.A8]					Global	0 mm:1 mm	2.8 mm	1.8 mm
PPr		U1.F14:U2.R3 [DDR.A9]					Global	0 mm:1 mm	5 mm	4 mm
PPr		U1.C15:U2.L7 [DDR.A10]					Global	0 mm:1 mm	5.4 mm	4.4 mm
PPr		U1.G11:U2.R7 [DDR.A11]					Global	0 mm:1 mm	5.8 mm	4.8 mm
PPr		U1.D16:U2.N7 [DDR.A12]					Global	0 mm:1 mm	3.8 mm	2.8 mm
PPr		U1.B15:U2.T3 [DDR.A13]					Global	0 mm:1 mm	0.8 mm	0.2 mm
PPr		U1.B16:U2.T7 [DDR.A14]					Global	0 mm:1 mm	3.4 mm	2.4 mm
PPr		U1.A14:U2.M7 [DDR.A15]					Global	0 mm:1 mm	5.6 mm	4.6 mm
PPr		U1.G14:U2.M2 [DDR.BA0]					Global	0 mm:1 mm	4.4 mm	3.4 mm
PPr		U1.G16:U2.N8 [DDR.BA1]					Global	0 mm:1 mm	1.6 mm	0.6 mm
PPr		U1.E16:U2.M3 [DDR.BA2]					Global	0 mm:1 mm	0.4 mm	0.6 mm
PPr		U1.K14:U2.K3 [DDR.CAS#]					Global	0 mm:1 mm	5 mm	4 mm
PPr		U1.G12:U2.J7 [DDR.CK]					Global	TARGET	TARGET	
PPr		U1.H14:U2.K1 [DDR.ODT]					Global	0 mm:1 mm	4.6 mm	3.6 mm
PPr		U1.J13:U2.J3 [DDR.RAS#]					Global	0 mm:1 mm	4.2 mm	3.2 mm
PPr		U1.F12:U2.T2 [DDR.RESET#]					Global	0 mm:1 mm	8.6 mm	7.6 mm
PPr		U1.E15:U2.L3 [DDR.WE#]					Global	0 mm:1 mm	0.2 mm	0.8 mm

Repeat these steps for U2>U3, U3>U4 AND U4>U5 as shown below:-

DDR_ADDR_CNTRL_DIMM2(25)
U2.N3:U3.N3 [DDR.A0]
U2.P7:U3.P7 [DDR.A1]
U2.P3:U3.P3 [DDR.A2]
U2.N2:U3.N2 [DDR.A3]
U2.P8:U3.P8 [DDR.A4]
U2.P2:U3.P2 [DDR.A5]
U2.R8:U3.R8 [DDR.A6]
U2.R2:U3.R2 [DDR.A7]
U2.T8:U3.T8 [DDR.A8]
U2.R3:U3.R3 [DDR.A9]
U2.L7:U3.L7 [DDR.A10]
U2.R7:U3.R7 [DDR.A11]
U2.N7:U3.N7 [DDR.A12]
U2.T3:U3.T3 [DDR.A13]
U2.T7:U3.T7 [DDR.A14]
U2.M7:U3.M7 [DDR.A15]
U2.M2:U3.M2 [DDR.BA0]
U2.N8:U3.N8 [DDR.BA1]
U2.M3:U3.M3 [DDR.BA2]
U2.K3:U3.K3 [DDR.CAS#]
U2.J7:U3.J7 [DDR.CK]
U2.K1:U3.K1 [DDR.ODT]
U2.J3:U3.J3 [DDR.RAS#]
U2.T2:U3.T2 [DDR.RESET#]
U2.L3:U3.L3 [DDR.WE#]

DDR_ADDR_CNTRL_DIMM3(25)
U3.N3:U4.N3 [DDR.A0]
U3.P7:U4.P7 [DDR.A1]
U3.P3:U4.P3 [DDR.A2]
U3.N2:U4.N2 [DDR.A3]
U3.P8:U4.P8 [DDR.A4]
U3.P2:U4.P2 [DDR.A5]
U3.R8:U4.R8 [DDR.A6]
U3.R2:U4.R2 [DDR.A7]
U3.T8:U4.T8 [DDR.A8]
U3.R3:U4.R3 [DDR.A9]
U3.L7:U4.L7 [DDR.A10]
U3.R7:U4.R7 [DDR.A11]
U3.N7:U4.N7 [DDR.A12]
U3.T3:U4.T3 [DDR.A13]
U3.T7:U4.T7 [DDR.A14]
U3.M7:U4.M7 [DDR.A15]
U3.M2:U4.M2 [DDR.BA0]
U3.N8:U4.N8 [DDR.BA1]
U3.M3:U4.M3 [DDR.BA2]
U3.K3:U4.K3 [DDR.CAS#]
U3.J7:U4.J7 [DDR.CK]
U3.K1:U4.K1 [DDR.ODT]
U3.J3:U4.J3 [DDR.RAS#]
U3.T2:U4.T2 [DDR.RESET#]
U3.L3:U4.L3 [DDR.WE#]

DDR_ADDR_CNTRL_DIMM4(25)
U4.N3:U5.N3 [DDR.A0]
U4.P7:U5.P7 [DDR.A1]
U4.P3:U5.P3 [DDR.A2]
U4.N2:U5.N2 [DDR.A3]
U4.P8:U5.P8 [DDR.A4]
U4.P2:U5.P2 [DDR.A5]
U4.R8:U5.R8 [DDR.A6]
U4.R2:U5.R2 [DDR.A7]
U4.T8:U5.T8 [DDR.A8]
U4.R3:U5.R3 [DDR.A9]
U4.L7:U5.L7 [DDR.A10]
U4.R7:U5.R7 [DDR.A11]
U4.N7:U5.N7 [DDR.A12]
U4.T3:U5.T3 [DDR.A13]
U4.T7:U5.T7 [DDR.A14]
U4.M7:U5.M7 [DDR.A15]
U4.M2:U5.M2 [DDR.BA0]
U4.N8:U5.N8 [DDR.BA1]
U4.M3:U5.M3 [DDR.BA2]
U4.K3:U5.K3 [DDR.CAS#]
U4.J7:U5.J7 [DDR.CK]
U4.K1:U5.K1 [DDR.ODT]
U4.J3:U5.J3 [DDR.RAS#]
U4.T2:U5.T2 [DDR.RESET#]
U4.L3:U5.L3 [DDR.WE#]

Using the same method create the pin pairs for the byte lanes. These also follow the fly by topology (so U1>U2>U3>U4>U5.

DDR_BYTE0_DIMM1(10)
U2.E3:U1.L14 [DDR.DQ0]
U2.F7:U1.L16 [DDR.DQ1]
U2.F2:U1.M15 [DDR.DQ2]
U2.F8:U1.M16 [DDR.DQ3]
U2.H3:U1.J14 [DDR.DQ4]
U2.H8:U1.J16 [DDR.DQ5]
U2.G2:U1.K15 [DDR.DQ6]
U2.H7:U1.K16 [DDR.DQ7]
U1.K11:U2.E7 [DDR.LDM]
U2.G3:U1.N16 [DDR.LDQS#]
DDR_BYTE0_DIMM2(10)
U3.E3:U2.E3 [DDR.DQ0]
U3.F7:U2.F7 [DDR.DQ1]
U3.F2:U2.F2 [DDR.DQ2]
U3.F8:U2.F8 [DDR.DQ3]
U3.H3:U2.H3 [DDR.DQ4]
U3.H8:U2.H8 [DDR.DQ5]
U3.G2:U2.G2 [DDR.DQ6]
U3.H7:U2.H7 [DDR.DQ7]
U2.E7:U3.E7 [DDR.LDM]
U3.G3:U2.G3 [DDR.LDQS#]
DDR_BYTE0_DIMM3(10)
U4.E3:U3.E3 [DDR.DQ0]
U4.F7:U3.F7 [DDR.DQ1]
U4.F2:U3.F2 [DDR.DQ2]
U4.F8:U3.F8 [DDR.DQ3]
U4.H3:U3.H3 [DDR.DQ4]
U4.H8:U3.H8 [DDR.DQ5]
U4.G2:U3.G2 [DDR.DQ6]
U4.H7:U3.H7 [DDR.DQ7]
U3.E7:U4.E7 [DDR.LDM]
U4.G3:U3.G3 [DDR.LDQS#]
DDR_BYTE0_DIMM4(10)
U5.E3:U4.E3 [DDR.DQ0]
U5.F7:U4.F7 [DDR.DQ1]
U5.F2:U4.F2 [DDR.DQ2]
U5.F8:U4.F8 [DDR.DQ3]
U5.H3:U4.H3 [DDR.DQ4]
U5.H8:U4.H8 [DDR.DQ5]
U5.G2:U4.G2 [DDR.DQ6]
U5.H7:U4.H7 [DDR.DQ7]
U4.E7:U5.E7 [DDR.LDM]
U5.G3:U4.G3 [DDR.LDQS#]

DDR_BYTE1_DIMM1(10)
U2.D7:U1.P15 [DDR.DQ8]
U2.C3:U1.P16 [DDR.DQ9]
U2.C8:U1.R15 [DDR.DQ10]
U2.C2:U1.R16 [DDR.DQ11]
U2.A7:U1.T14 [DDR.DQ12]
U2.A2:U1.T13 [DDR.DQ13]
U2.B8:U1.R12 [DDR.DQ14]
U2.A3:U1.T12 [DDR.DQ15]
U1.K12:U2.D3 [DDR.UDM]
U2.B7:U1.T15 [DDR.UDQS#]
DDR_BYTE1_DIMM2(10)
U3.D7:U2.D7 [DDR.DQ8]
U3.C3:U2.C3 [DDR.DQ9]
U3.C8:U2.C8 [DDR.DQ10]
U3.C2:U2.C2 [DDR.DQ11]
U3.A7:U2.A7 [DDR.DQ12]
U3.A2:U2.A2 [DDR.DQ13]
U3.B8:U2.B8 [DDR.DQ14]
U3.A3:U2.A3 [DDR.DQ15]
U2.D3:U3.D3 [DDR.UDM]
U3.B7:U2.B7 [DDR.UDQS#]
DDR_BYTE1_DIMM3(10)
U4.D7:U3.D7 [DDR.DQ8]
U4.C3:U3.C3 [DDR.DQ9]
U4.C8:U3.C8 [DDR.DQ10]
U4.C2:U3.C2 [DDR.DQ11]
U4.A7:U3.A7 [DDR.DQ12]
U4.A2:U3.A2 [DDR.DQ13]
U4.B8:U3.B8 [DDR.DQ14]
U4.A3:U3.A3 [DDR.DQ15]
U3.D3:U4.D3 [DDR.UDM]
U4.B7:U3.B7 [DDR.UDQS#]
DDR_BYTE1_DIMM4(10)
U5.D7:U4.D7 [DDR.DQ8]
U5.C3:U4.C3 [DDR.DQ9]
U5.C8:U4.C8 [DDR.DQ10]
U5.C2:U4.C2 [DDR.DQ11]
U5.A7:U4.A7 [DDR.DQ12]
U5.A2:U4.A2 [DDR.DQ13]
U5.B8:U4.B8 [DDR.DQ14]
U5.A3:U4.A3 [DDR.DQ15]
U4.D3:U5.D3 [DDR.UDM]
U5.B7:U4.B7 [DDR.UDQS#]

Another useful Electrical Constraint is a Wiring constraint to verify that the net(s) in question are routed the way you want them to be. For this design use Edit>Net Schedule, then pick each net and select the path you want to route it on. This creates a User Defined schedule (Constraint Manager>Electrical>Net>Routing>Wiring worksheet) which can then have a Verify set to Yes to confirm that you follow this topology. You can also define a maximum stub length (fanout via distance). In this example all the nets have been manually scheduled, if you have access to Allegro PCB Designer you can schedule one net then make an ECSet from that and apply it to all the other nets. If you have access to Allegro PCB Designer + High Speed, then this can all be achieved within SigExplorer and applied directly to the design. (Address bus shown only for information).

ADDRESS(16)		Yes				0.5000
DDR.A0		Yes	User Defined	PASS		0.5000
DDR.A1		Yes	User Defined	PASS		0.5000
DDR.A2		Yes	User Defined	PASS		0.5000
DDR.A3		Yes	User Defined	PASS		0.5000
DDR.A4		Yes	User Defined	PASS		0.5000
DDR.A5		Yes	User Defined	PASS		0.5000
DDR.A6		Yes	User Defined	PASS		0.5000
DDR.A7		Yes	User Defined	PASS		0.5000
DDR.A8		Yes	User Defined	PASS		0.5000
DDR.A9		Yes	User Defined	PASS		0.5000
DDR.A10		Yes	User Defined	PASS		0.5000
DDR.A11		Yes	User Defined	PASS		0.5000
DDR.A12		Yes	User Defined	PASS		0.5000
DDR.A13		Yes	User Defined	PASS		0.5000
DDR.A14		Yes	User Defined	PASS		0.5000

Routing the design

Once the rules are set (and remember this is just an example of a DDR fly-by topology). You are now ready to start routing the design. This can be done either manually or automatically using the OrCAD Designer Professional autorouter. In this example though the routing was completed manually using four routing layers, TOP, INNER1, INNER2 and BOTTOM, leaving a dedicated GND plane and a Split power plane for DDR_VDD and DDR_VDD. To improve impedance and limit crosstalk you may want to route the majority of the DDR routes onto inner layers. When routing remember to leave enough room between the traces to allow for length matching patterns such as accordion and trombone. The automatic tools (AiDT and AiPT available from Allegro + High Speed) will spread the routing but try and allow for this if possible. You can get an idea about how much room you need from the screenshots in the next few pages.

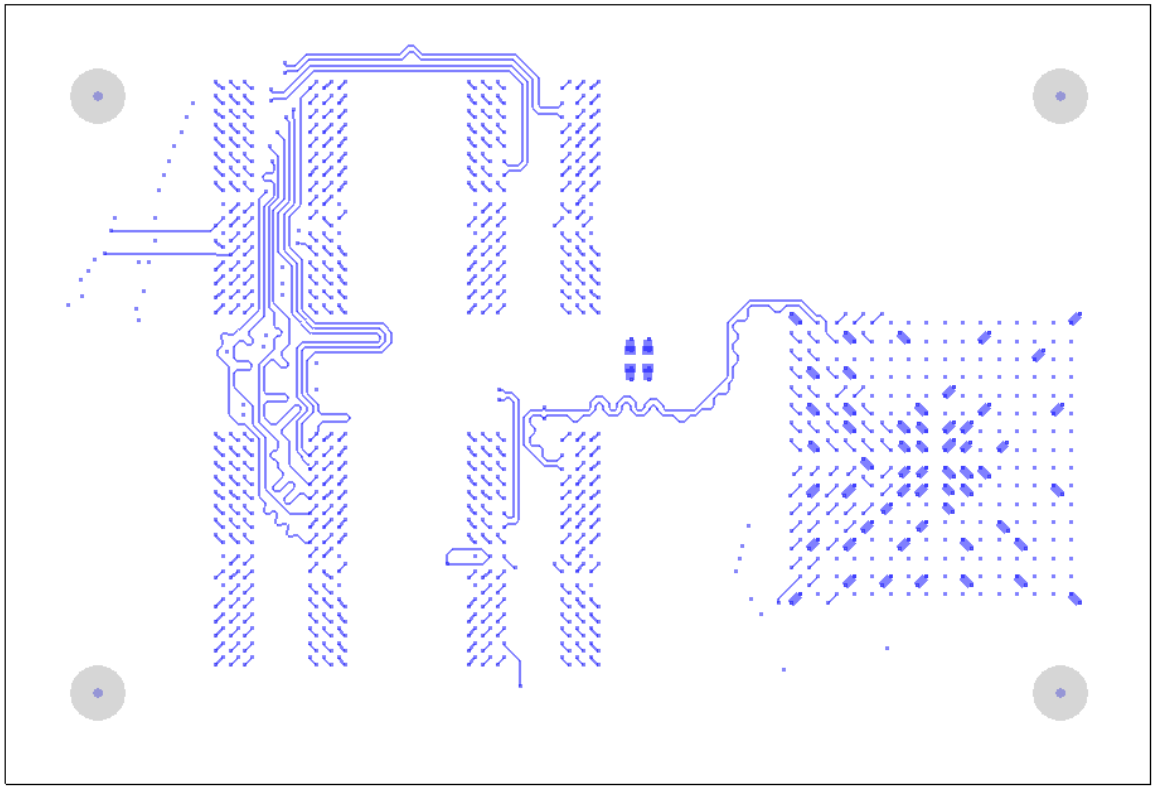
Once the basic routing has been added you could if you have access use the Allegro PCB Designer + High Speed option and use tools such as Timing Vision and Auto Interactive Delay and Phase tuning to match the lengths of the match groups defined. If you don't have access to these you can still achieve the results using Delay and Phase Tuning, it just might take longer.

You can download the actual OrCAD/Allegro board file. In the PDF look at the Attachments icon then right click – Save Attachment and save the board file locally.

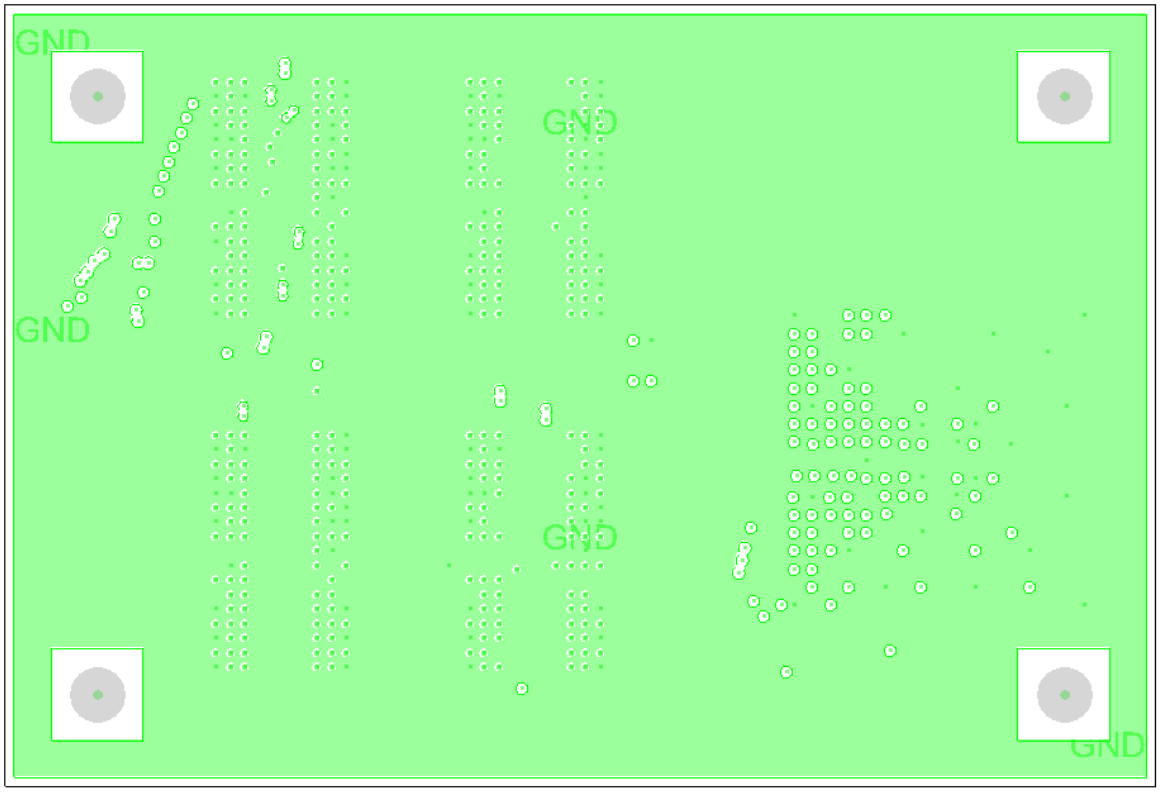
PCB Layers

Below are screenshots of each layer of the PCB to give you an idea of the routing.

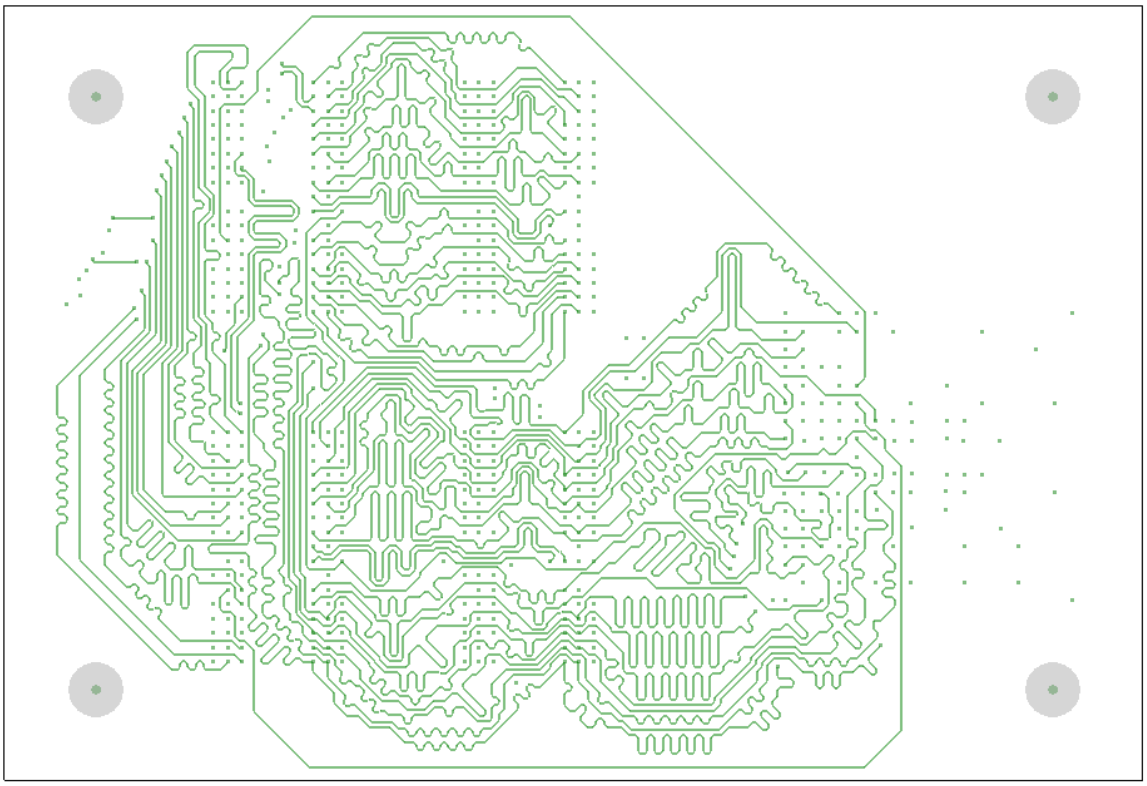
TOP



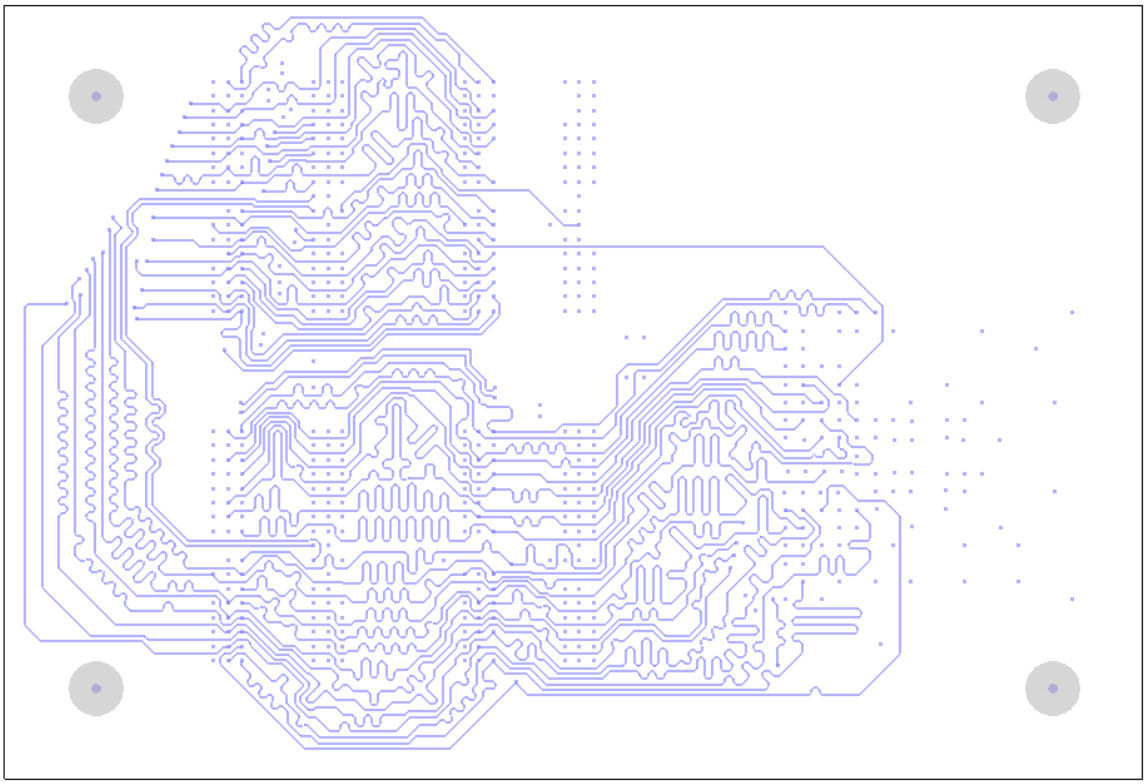
GND



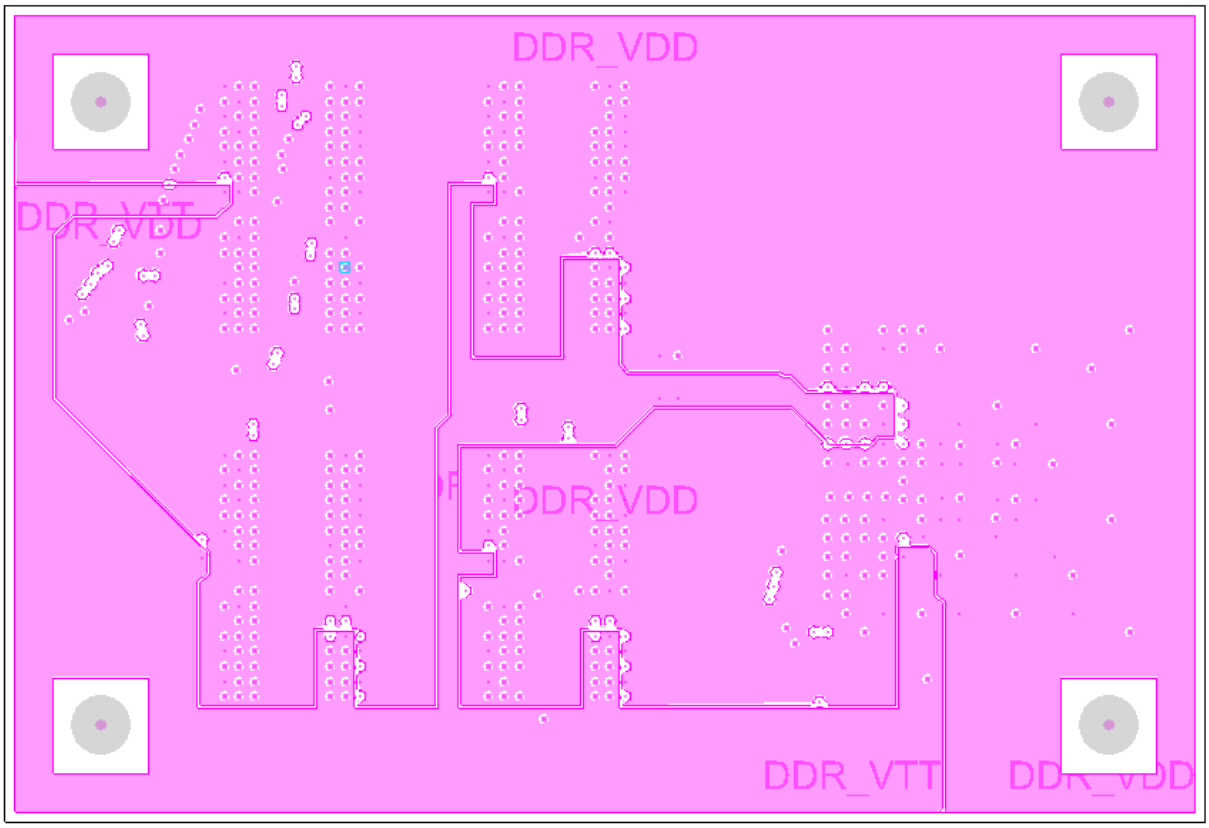
INNER1



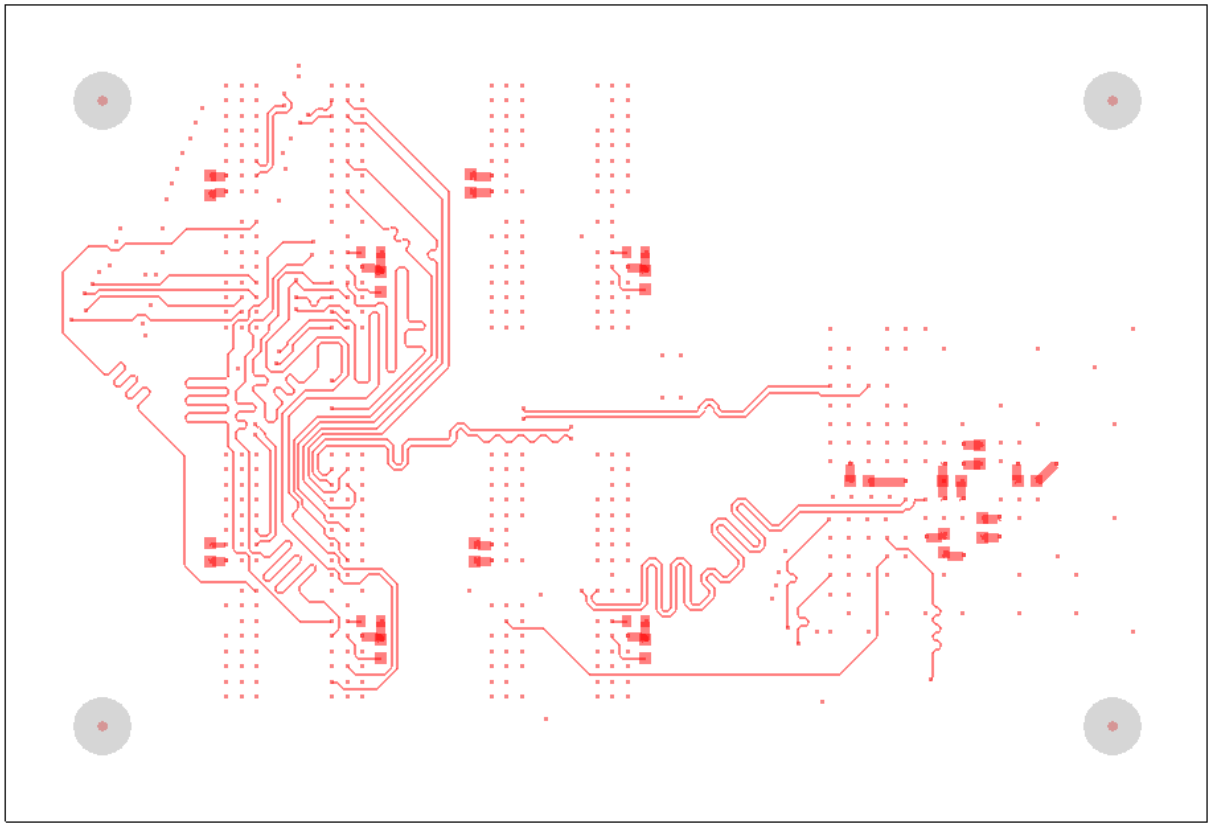
INNER2



POWER



BOTTOM



Considerations

There are some instances in this design where some of the design rules may have been tweaked to allow for a successful route. Differential Pair uncoupled length is one example where a decision to match the differential pair lengths to meet the criteria was made over the differential pair being uncoupled longer for certain sections of the routing. That may/may not be the correct decision, but these are choices you can make on your own designs.

DPr		DP_UDQS	DIFFPAIR			Ignore		16.1000		0.0205
Net		DDR.UDQS	DIFFPAIR			Ignore		16.1000		0.3820
RePP		U5.C7:U1.R14				Ignore	2.2820	16.1000	15.7180	0.3820
Net		DDR.UDQS#	DIFFPAIR			Ignore		16.1000		0.0205
RePP		U5.B7:U1.T15				Ignore	0.6899	16.1000	16.0795	0.0205

The same can also be said for Stub length where a default fanout via may have been moved to improve routing channels.

DPr		DP_CK	DIFFPAIR	Yes				0.6000
Net		DDR.CK	DIFFPAIR	Yes	User Defined	PASS		0.6000
Net		DDR.CK#	DIFFPAIR	Yes	User Defined	PASS		0.6000
DPr		DP_LDQS	DIFFPAIR	Yes				9.0000
Net		DDR.LDQS	DIFFPAIR	Yes				9.0000
Net		DDR.LDQS#	DIFFPAIR	Yes				9.0000
DPr		DP_UDQS	DIFFPAIR	Yes				6.0000
Net		DDR.UDQS	DIFFPAIR	Yes				22.0000
Net		DDR.UDQS#	DIFFPAIR	Yes				22.0000