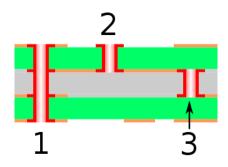


How to Define Blind and Buried Vias

Introduction

Many PCB's used in today's market have real estate restrictions, meaning less room is available for routing and vias. Designers get round this problem using Blind and Buried Vias. The three types of standard vias are shown in the figure below. 1 is a Through Via, 2 is a Blind Via and 3 is a Buried via. Blind and buried vias will save room because the holes do not extend through the whole PCB. The downside to using this technology is increased cost during manufacture of the bare board.



How to define a Blind and Buried Vias.

PCB Editor uses standard through hole vias as a basis for any blind / buried vias. A via is a standard padstack normally named via for ease of use during Constraint Manager setup. They are stored in the padpath location and can then be added to any design database.

To setup a Blind or Buried via firstly ensure that the stack-up or cross section of the PCB has been defined, then use Setup > B/B Via Definitions > Define B/B Via (Allegro) or Setup > Define B/B Vias (OrCAD). The following GUI appears: -

| 🎛 Blind / Buried Vias | | | - | | × |
|-----------------------|------------------|-------------|-----------|--|---|
| BBVia Padstack | Padstack to Copy | Start Layer | End Layer | | |
| Delete | VIA | • | | | - |
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| OK Cancel | Add BBVia Help | | | | |
| | | | | | |

BBVia Padstack - Indicates the name of the blind / buried via, you can call these want you want, it can be recommended that part of the name includes the start / end layers e.g. bbvia_l1_l2 (a blind via from Layer1 to Layer2).

Padstack to Copy - Indicates the name of the padstack you are copying from the library from which the new via is created. The button to the right of the Padstack to Copy field displays a data browser containing a list of available database/library padstacks.

Start Layer - Displays a pop-up list of the etch layers in the design. Choose the name of the etch layer that begins the new padstack.

End Layer - Displays a list of the etch layers in the design. Choose the name of the etch layer that ends the new padstack.

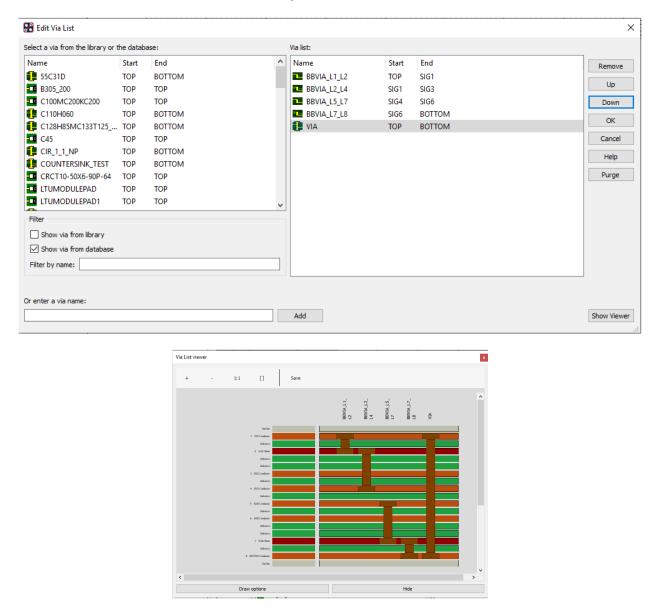
The following screenshot shows two Blind and two Buried vias and the via padstack name they are based on. The start and end layers signify which layers they start and finish on.

| 🔡 Blind / Bu | ried Vias | | | | | _ | | \times |
|--------------|-------------|----------------|----|---------|--------|---------|----|----------|
| BBV | ia Padstack | Padstack to Co | ру | Start L | ayer | End Lay | er | |
| Delete | BBVIA_L5_L7 | VIA | | SIG4 | - | SIG6 | | - |
| Delete | BBVIA_L2_L4 | VIA-0_3-0_15 | | SIG1 | - | SIG3 | | - |
| Delete | BBVIA_L7_L8 | VIA-0_45-0_2 | | • | BOTTOM | | | |
| Delete | BBVIA_L1_L2 | VIA-0_45-0_2 | | TOP | - | SIG1 | | • |
| | | | | | | | | |
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| | | | | | | | | |
| ОК | Cancel | Add BBVia | He | łp | | | | |
| | | | | | | | | |

Once the bb vias have been defined they need to be added to the Physical Constraint Sets in Constraint Manager the same as you would add a through hole via. Launch Constraint Manager, Setup > Constraints > Constraint Manager (Allegro) or Setup > Constraints (OrCAD) then go to Physical Constraint Set > All Layers

| Flectrical | | Objects | | | | Line Width | | Neck | | Differential Pair | | | | | |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|---------|-------|--------------|-----------------------------|------------|-------|----------------------|-------|--------------------------------|-------|----------|--------------|--------------|------|
| → | | | s | Name | Referenced Physical CSet | Min Max | | Min Width Max Length | | Min Line Spacing Primary Ga | | Neck Gap | (+)Tolerance | (-)Tolerance | Vias |
| All Layers | " | pe | | Name | | mm | mm | mm | mm | mm | mm | mm | mm | mm | |
| ✓ Image: Vector vec | · | | • | * | • | • | • | • | • | • | • | • | • | • | * |
| V 🗎 Region | Ds | | | DEMOP-placed | DEFAULT | | | 0.150 | 2.500 | | | 0.000 | 0.000 | | VIA |
| All Layers | PC | S | ***** | DEFAULT | | 0.200 | 0.000 | 0.150 | 2.500 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | VIA |

Click on the VIA in the Vias column. The newly defined BB Vias will be available in the Top Left Hand List. Double Click each one to move it into the Via List on the right hand side.



The vias are graphically displayed on the viewer (shown undocked) showing the layers that they span. The order of the via list is **important**. If VIA which is a through hole via is at the top of the ViaList then PCB Editor will always use this via by default because it can resolve any routing requirement from and to any layer, so it is recommended that the via list follow the order of the PCB stackup. The display above shows a good example of this. Click Ok and the vias are now available for use.

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