Introduction

Microvias are a principal feature of HDI, defined by the IPC as vias whose diameter is less than approx. 0.15mm with capture pads less than 0.35mm. Microvias set up the clearance matrix associated with the technology, such as microvia-to-microvia and microvia-to-core via spacing rules. Prior to 16.2, all non-standard vias (buried and blind) were categorized by the database object BB Via. Allegro PCB Editor + Miniaturization Option lets you differentiate microvias from mechanically drilled blind and buried vias using the Microvia option on the Padstack Editor. Microvias are commonly used in stack-ups similar to the one shown in figure 1 courtesy of IPC 2226. This stack-up is probably the most commonly used stack-up used in the industry for HDI Design. Cost efficiency is achieved by limiting both the number of laminations and use of stacked vias. As package pitch continues to decrease, the used of stacked Microvias or stacked Micro to Core vias may become more common.

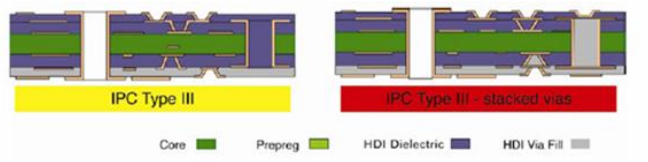
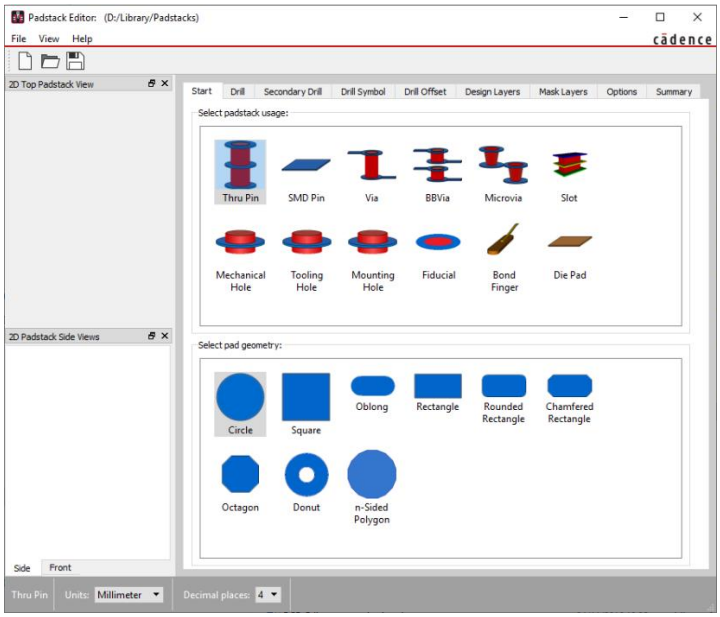


Figure 1 – HDI Type III Stack-up

While PCB Editor currently supports B/B Vias, the newly established Microvia is necessary to setup the clearance matrix associated with the technology. This includes but not limited to “Microvia to Microvia” and “Microvia to Core Via” spacing rules. Prior to 16.2, all non-standard vias (buried and blind) were categorized by the database object “BB Via”. In addition, the Same Net DRC system was not robust enough to differentiate net to net from same net spacing rules; specifically, the Same Net system derives its values from the Net to Net rules.

Microvia Padstack

The Padstack Editor now supports a “Microvia” Usage option. This option is limited to B/B via types and is primarily used to drive HDI spacing rules between it and other metal objects in both the Spacing and the Same Net Spacing domains in Constraint Manager.



Usage Options

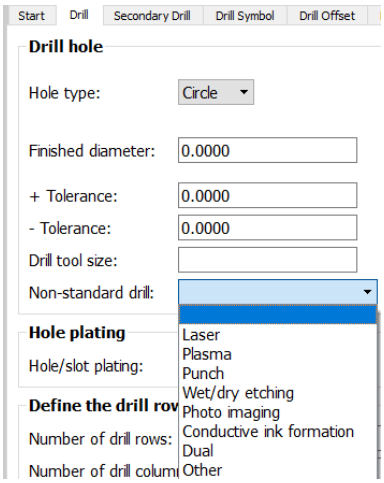
Two usage options can be associated with the padstack.

- **Microvia** – Use on HDI boards where spacing rule sets differ between HDI and conventional blind and buried or core vias. The Microvia option can only be applied to a blind and buried via to represent mechanical drilled vias, such as the core via on an HDI design. The Spacing and Same Net Spacing Constraint domains of Constraint Manager support these two via types
- **Allow Suppression of Unconnected Internal Pads** – Enable to suppress unused inner layer pads, thereby making them unavailable for DRC, routing, and display, with the Suppress Unconnected Pads option on the Film Control tab of the Artwork Control Form, available by choosing Manufacturing – Artwork or with dynamic unused pad suppression, available by choosing Setup – Cross Section.

Non Standard Drill Types

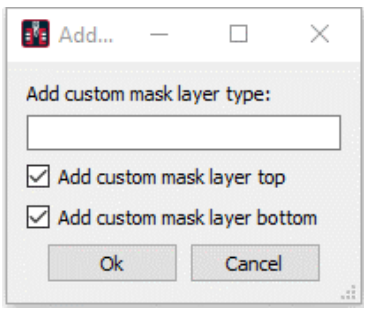
The Padstack Editor supports the following list of Non-standard drill types, most of which are used for HDI vias. These drill types are exclusively used with NC Drill applications and do not contribute toward Design Rule Checks. Use these non-standard types if you wish to separate those drills into their own individual files.

- Laser
- Plasma
- Punch
- Wet/Dry Etching
- Photo Imaging
- Conductive Ink Formation
- Dual
- Other



User Definable Mask Layers

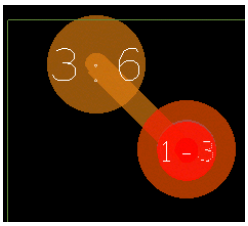
The Padstack Editor supports up to 16 user-definable mask layer pairs (Maximum of 32 layers total). Mask layers can be used for custom applications such as via plugging, filling, gold deposition to name a few. DRCs are not performed on these layers. Click the Add Layers button on the Mask Layers tab then enter the Mask Layer Name.



B/B Via Span Labels

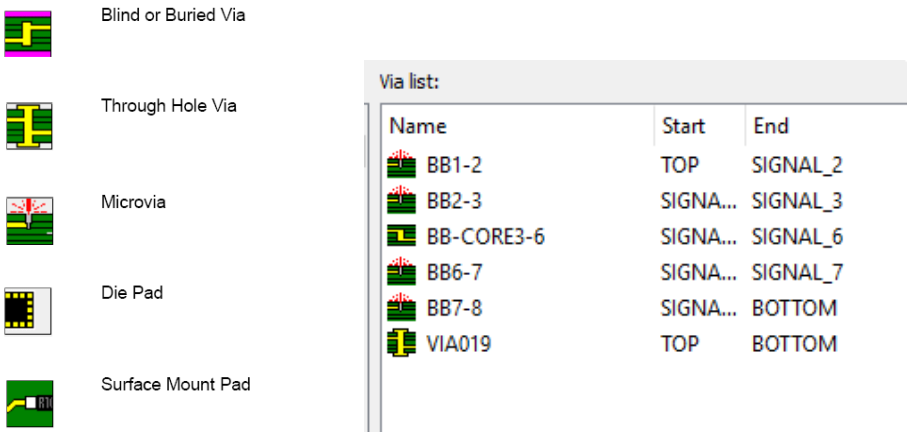
Via span labels graphically identify the beginning and ending layers of a single via or a series of stacked vias using the layer ID's within the pad extents. A colon between the beginning and ending layers indicates the span of a single blind and buried via; a dash represents a stacked series of blind and buried vias. Enable via span labels using

the Display tab of the Design Parameter Editor, available by choosing Setup > Design Parameters. The label's color defaults to white, but is customizable through the Display tab of the Color dialog box, available by choosing Display > Color/Visibility (Allegro) or Setup > Colors (OrCAD). Layer numbers ascend in numerical sequence; for example, Layer Top = 1, Inner Layer 1 = 2, Plane 1 = 3 by default or is customizable using a 3 alpha-numeric character limit set within the Cross Section Editor, Physical section, Setup > Cross Section. Labels do not appear on through-hole vias or pins.



Via List Enhancements

The Via List, an object in the Physical Constraint Set, supports bitmaps and Start/End layer fields to identify the via type and its range. The list represents a selectable order of vias when used with Route > Add Connect command. For example, the graphic below suggests BB1-2 be the priority via when transitioning from Layer Top to Signal_2; the alternative being the thru-hole via VIA019.



Same Net DRC Overview

Using the Same Net Spacing domain in Constraint Manager, the Same Net DRC system drives many rules for via tangency (vias that touch) and inset (vias that overlap) used on HDI designs. Each Spacing DRC has a respective Same Net DRC whose values can be set independently of Net to Net Spacing DRCs. For example, a Via to Pin rule can now be set to 0.15mm Net to Net and 0.075mm for Same Net. Same Net DRC error codes are a lower-case version of those for Net to Net. Same Net DRC modes can also be set on an individual basis. Spacing differentiation is available for the following via combinations:

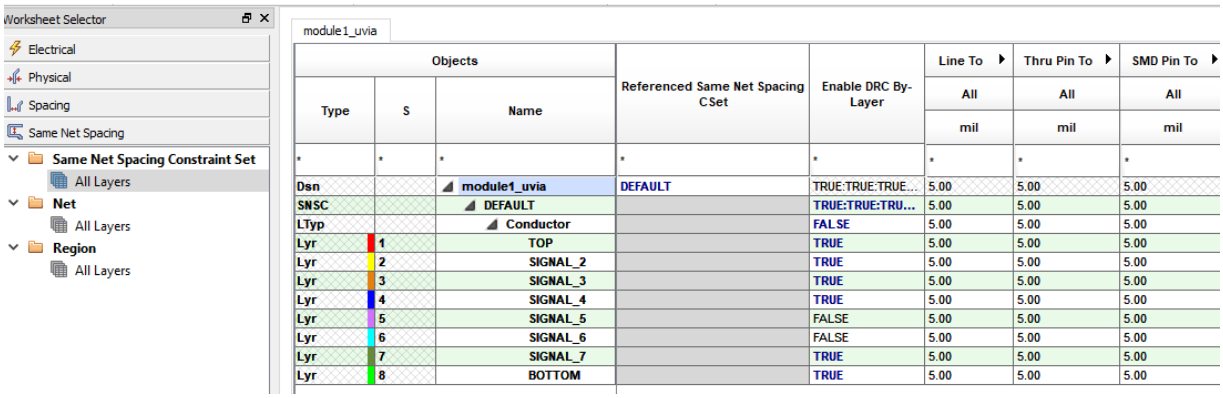
- Microvia to Microvia
- Microvia to Core Via (represented as blind and buried Via)
- Microvia to Thru-hole
- Core Via to Core Via
- Core Via to Thru-hole

Etch edit applications align with the changes made to the Same Net DRC system, including bubbling, which makes sliding vias to other vias or pins on the same net more efficient. The add-via model adds via structures while

obeying Same Net rules. Physical domain settings control stacking, and stacked vias are seen as a group entity with options for breaking the stack when necessary.

Constraint Manager – Same Net Spacing Domain

Same Net Spacing rules are managed entirely within the Same Net Spacing domain in Constraint Manager. An equivalent Same Net DRC represents each Spacing DRC. The Same Net domain is structured similarly to the Spacing domain, in terms of constraint inheritance and overrides. Constraint objects unsupported in the domain are Net Class-Class and Region Class-Class, as they are used exclusively for net-net rules.



Objects			Referenced Same Net Spacing CSet	Enable DRC By-Layer	Line To	Thru Pin To	SMD Pin To
Type	S	Name			All	All	All
					mil	mil	mil
*	*	*	*	*	*	*	*
Dsn		module1_uvia	DEFAULT	TRUE:TRUE:TRUE...	5.00	5.00	5.00
SNSC		DEFAULT		TRUE:TRUE:TRU...	5.00	5.00	5.00
LTyp		Conductor		FALSE	5.00	5.00	5.00
Lyr	1	TOP		TRUE	5.00	5.00	5.00
Lyr	2	SIGNAL_2		TRUE	5.00	5.00	5.00
Lyr	3	SIGNAL_3		TRUE	5.00	5.00	5.00
Lyr	4	SIGNAL_4		TRUE	5.00	5.00	5.00
Lyr	5	SIGNAL_5		FALSE	5.00	5.00	5.00
Lyr	6	SIGNAL_6		FALSE	5.00	5.00	5.00
Lyr	7	SIGNAL_7		TRUE	5.00	5.00	5.00
Lyr	8	BOTTOM		TRUE	5.00	5.00	5.00

The table below indicates the hierarchy used to manage the Electrical, Physical and Spacing rules.

	Electrical	Physical	Spacing (net-to-net / same-net)
INHERITANCE	----------	Design	Design
	Net Class	Net Class	Net Class
	Bus	Bus	Bus
	Differential Pair	Differential Pair	Differential Pair
	Match/Relative Group	----------	----------
	Xnet	Xnet	Xnet
	Net	Net	Net
	Pin Pair	Pin Pair	Pin Pair
	----------	----------	Net Class-Class *
	----------	Region	Region
	----------	Region Class	Region Class
	----------	----------	Region Class-Class *

OVERRIDE

* Not available in the Same Net Spacing domain

Etch Edit Support for Same Net Rules

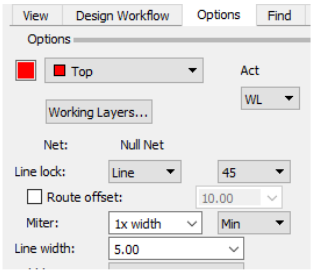
Etch-editing integrates the bubble code (shove/hug) to allow it to work with certain Same Net conditions. Sliding HDI vias in proximity with other vias or pins is more efficient due to the adherence of Same Net rules. Other enhancements include:

- Sliding of via stacks as a single entity
- Splitting the stack (etch now connected to via, previously orphaned)

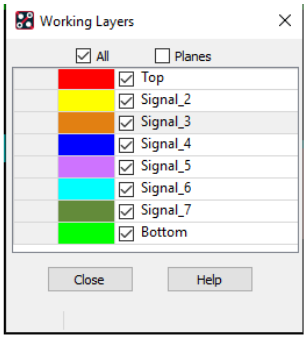
- Sliding a via, then snapping it into a stack if rules permit
- Adding HDI via structures while obeying Same Net Rules during insert
- Staggered, Stacked, and Inset
- Sliding of vias from pad will maintain etch connection (previously orphaned)

HDI Via Structures

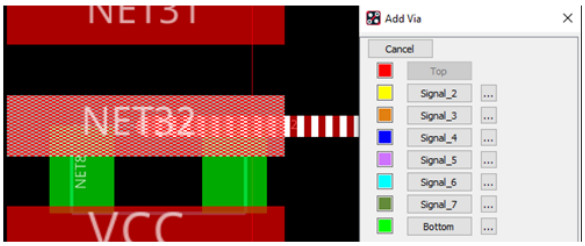
This methodology to add both conventional and HDI via structures includes a working layer model based on the concept of multiple alternate layers, in conjunction with a via popup interface. Double-clicking in the canvas displays the Via Popup interface, populated by the layers enabled in the Working Layer Setup dialog box that displays along with access to the via list. This combination automates the sequence of layer transitions using stacked, staggered, and inset vias by localizing the steps of layer transition near the point of occurrence to maintain focus on the working board area, limiting travel to side panels or to the toolbar during routing. Metrics can be established to measure increased productivity and efficiency, relative to the number of mouse clicks to complete a connection.



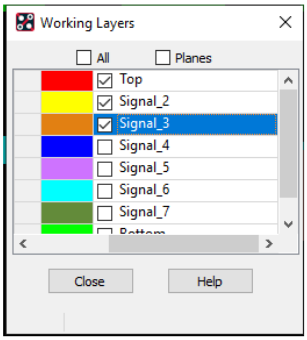
Enable WL Mode



Enable Working Layers



Vi Popup GUI



Reduce number of Working Layers

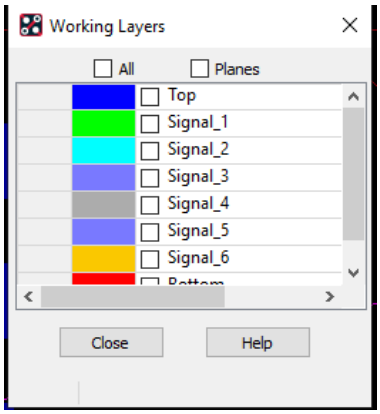
Proportional Via Popup List

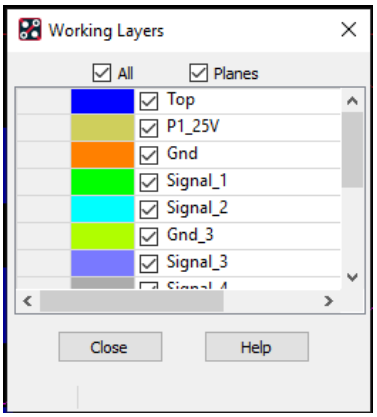
Working Layer Dialog

With the Add Connect command active, access the Working Layer dialog from the:

- Options Panel (right side of canvas)
- Right click > Working Layers menu selection

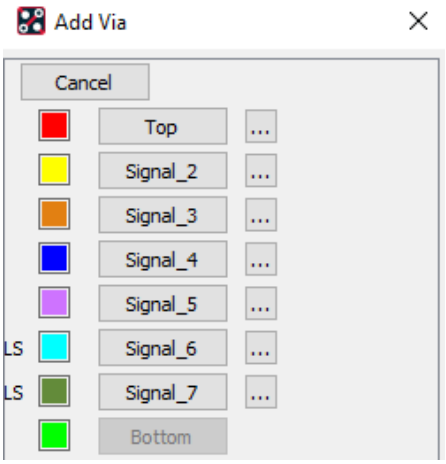
The color swatches that appear in the form align with the colours used for the ETCH subclasses. Plane layer display is an available option when enabled appends all layers classified as PLANE to the list. By default, Plane layer display disabled since it's uncommon to route on them.





Layer Set Identification

It is not necessary to keep the Working Layer form open during routing however the following behaviour should be noted when routing nets constrained by Layer Set rules. The first column of the dialog is reserved for LS (Layer Set) identification. Similar to the bolding of layers in the legacy add via model, LS appears adjacent to all layers of the Layer Set definition. These layers will become temporarily enabled if in a disabled state.

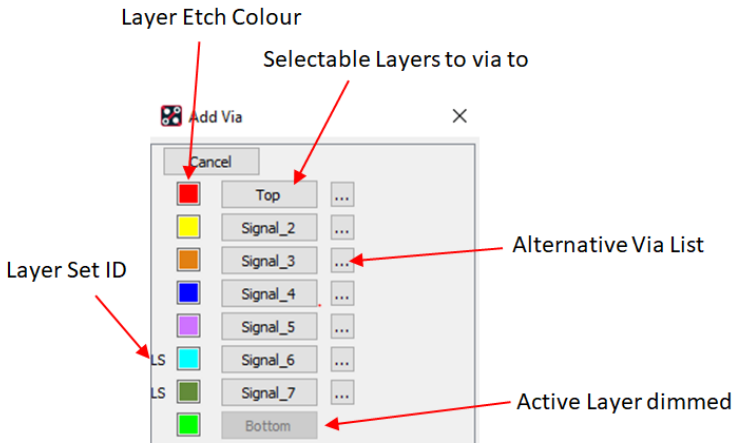


Via Popup GUI

When the 'Working Layer' Mode is enabled, a Left double-click produces a Via Popup GUI at about the location of the via to be inserted. The layers that populate the GUI are driven from the 'Working Layer' setup form with the Active layer always dimmed out. When only 2 layers are enabled, a LMB double-click adds the via without GUI intervention. This emulates the legacy Active/Alternate model.

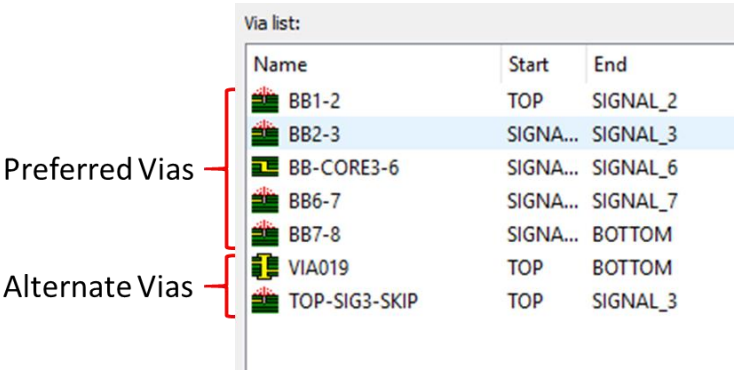
The via(s) inserted are driven by the ordering in the respective Physical CSets. This is discussed more in the next section. The ellipse buttons on the right side of the form provide access to alternate or least preferred vias based on the ordering within the Physical CSet.

One of the major benefits of this model is the ability to automatically add sequential B/B vias on the path to the destination layer. If stacking rules are permitted, each via of the stack is added at a coincident location. If stacking is not permitted and staggering rules prevail, each via of the sequence is floated on your cursor spiralling around the previously instantiated via at 22.5 degree increments with respect to the same net spacing rule between the 2 via types.



Ordered Via List

An ordered via list lets you select the target layer to which to route while PCB Editor populates the preferred vias in the layer series. In Working Layers mode, you must have predefined vias in the constraint set via list for the layers upon which you want to route; however, this mode assumes that you have defined an "ordered via list" for Physical CSets in Constraint Manager. The vias listed in the Edit Via List are available for adding when you route interactively.



Stacked HDI Vias

A via stack comprises two or more Same-Net vias that are directly connected at the same location, with adjacent vias in the stack each sharing one common layer. A Split Stack option available from a right-mouse popup menu allows one or more vias to be split from their via stack if required. When sliding a via (or stack of vias) outside the pin pad, a cline is added as necessary to avoid orphan vias, or those that become disconnected from the net.

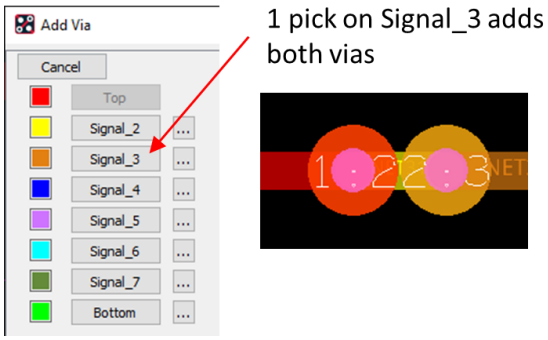
Staggered HDI Vias

A microvia on one layer connecting to a via on the second layer can be staggered or offset such that the pad diameters are tangential or greater when vias are not allowed to be stacked.

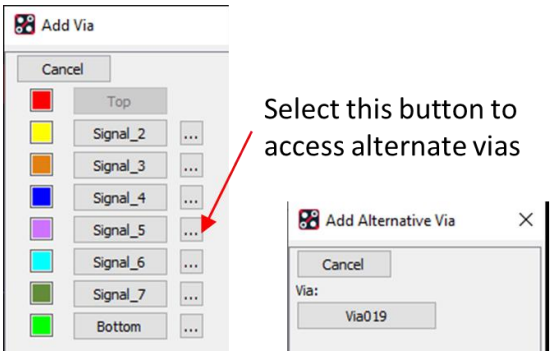
Example

Using the Via List in the above graphic, a signal is being routed on Layer Top.

- A LMB double click produces the Via Pop GUI shown below.
- Signal_3 is selected from the list, form closes.
- BB1-2 is inserted at pick point; BB2-3 via spirals around BB1-2 @ 22.5 degree increments.



Using the same example, instead of selecting Signal_3, the ellipse button adjacent to it is selected producing the list of alternate vias to choose from. Selection of either via from the list closes the form and adds the via.



Adding HDI Vias

The new add via model is designed to increase the efficiency of adding HDI vias of the following structure types

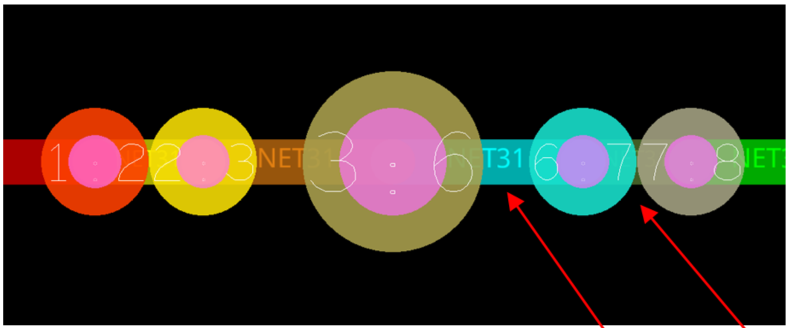
- Staggered
- Stacked Microvias/Offset Core Via
- Stacked Microvia & Core Via
- Inset Vias (Overlapping of vias)
- Any Layer Via

The add via model is based on the selection of the destination layer in combination with the appropriate Physical CSet driven ordered Via List. In the 4 examples below, a transition is made from Layer Top to Bottom.

Example 1 – Adding Staggered Vias

The following vias are used in the sequence (BB1-2, BB2-3, BB3-6, BB6-7, BB7-8). All but BB3-6 are classified as Microvias.

- While routing on Layer Top (1), a Left double-click produces the Via Popup GUI where Layer Bottom (8) is selected.
- BB1-2 via is inserted at the pick location; BB2-3 is floating on the cursor.
- Remaining vias are semi-automatically added where user has control of location about the previously inserted via.
- Rotation angle about previously inserted via is 22.5 degrees.
- Use CNTL key to go into free angle mode if desired.
- Separation of vias is controlled by the Same Net rules for Microvia to Microvia (0 mils) and Microvia to BB Via (0.127mm)

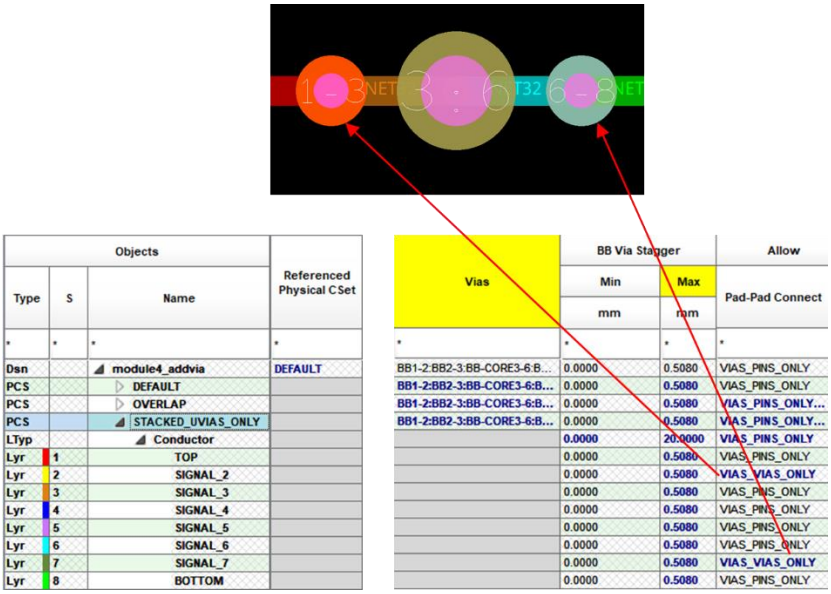


Objects				Microvia To										
Type	S	Name	Referenced Same Net Spacing CSet	All	Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Microvia	Shape	Bond Finger
				mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm
*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
Dsn		module4_addvia	DEFAULT	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270
SNSC		OVERLAP		0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270
SNSC		DEFAULT		0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270
LTyp		Conductor		0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270
Lyr	1	TOP		0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270
Lyr	2	SIGNAL_2		0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270
Lyr	3	SIGNAL_3		0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270
Lyr	4	SIGNAL_4		0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270
Lyr	5	SIGNAL_5		0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270
Lyr	6	SIGNAL_6		0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270
Lyr	7	SIGNAL_7		0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270
Lyr	8	BOTTOM		0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270

Example 2 – Adding Stacked Microvias

Similar to Example 1, the following vias are used in sequence (BB1-2, BB2-3, BB3-6, BB6-7, BB7-8) however in this example, rules permit the stacking of BB1-2 to BB2-3 and BB6-7 to BB7-8. The Core via (BB3-6) is offset from the stacked vias.

- While routing on Layer Top (1), a Left double-click produces the Via Popup GUI where Layer Bottom (8) is selected.
- Both BB1-2 and BB2-3 vias are inserted coincidently (at same x,y location) at the pick location; BB3-6 via is now floating on cursor.
- Physical CSet rules to allow stacking include:
  - Min BB Stagger set to 0
  - Allow Pad to Pad Connect set to Vias_Vias_only on Layers Signal_2 and Signal_7.
- BB3 Label associated with stack provides guidance that more than 1 set of B/B vias are stacked (label 1-3).-6 separation from the stacked Microvias is controlled by the Same Net Microvia to BB Via rule of 0.127mm.
- 1 Left click inserts BB3-6 via; BB 6-7 and BB7-8 (stacked formation) floating on cursor, separation to BB3-6 controlled by Same Net Microvia to BB Via rule of 5 mils.
- 1 Left click inserts both BB6-7 and BB7-8 at the pick location.
- The slide command treats the stacked vias as a single entity. Use the right click > Split Stack command to slide a specific via of the stack.



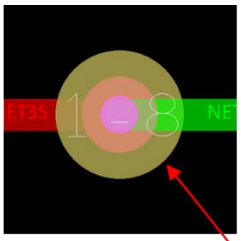
Objects			Referenced Physical CSet
Type	S	Name	
*	*	*	*
Dsn		module4_addvia	DEFAULT
PCS		DEFAULT	
PCS		OVERLAP	
PCS		STACKED_UVIAS_ONLY	
LTyp		Conductor	
Lyr	1	TOP	
Lyr	2	SIGNAL_2	
Lyr	3	SIGNAL_3	
Lyr	4	SIGNAL_4	
Lyr	5	SIGNAL_5	
Lyr	6	SIGNAL_6	
Lyr	7	SIGNAL_7	
Lyr	8	BOTTOM	

Vias	BB Via Stagger		Allow
	Min	Max	Pad-Pad Connect
	mm	mm	
*	*	*	*
BB1-2:BB2-3:BB-CORE3-6:B...	0.0000	0.5080	VIAS_PINS_ONLY
BB1-2:BB2-3:BB-CORE3-6:B...	0.0000	0.5080	VIAS_PINS_ONLY
BB1-2:BB2-3:BB-CORE3-6:B...	0.0000	0.5080	VIAS_PINS_ONLY...
BB1-2:BB2-3:BB-CORE3-6:B...	0.0000	0.5080	VIAS_PINS_ONLY...
	0.0000	20.0000	VIAS_PINS_ONLY
	0.0000	0.5080	VIAS_PINS_ONLY
	0.0000	0.5080	VIAS_VIAS_ONLY
	0.0000	0.5080	VIAS_PINS_ONLY
	0.0000	0.5080	VIAS_PINS_ONLY
	0.0000	0.5080	VIAS_PINS_ONLY
	0.0000	0.5080	VIAS_PINS_ONLY
	0.0000	0.5080	VIAS_VIAS_ONLY
	0.0000	0.5080	VIAS_PINS_ONLY

Example 3 – Adding Stacked Micro/Core Vias

The following vias are used in sequence (BB1-2, BB2-3, BB3-6, BB6-7, BB7-8) however in this example, rules permit the stacking of all via types.

- While routing on Layer Top (1), a Left double-click produces the Via Popup GUI where Layer Bottom (8) is selected.
- The entire set of vias are inserted at the pick point.
- The via label is indicative of the complete stacked series of vias (1-8)
- Physical CSet rules to allow stacking include:
  - Min BB Stagger set to 0
  - Allow Pad to Pad Connect set to Vias_Vias_only on all layers except Top and Bottom where settings support Via-in-Pad.
- The slide command treats the stacked vias as a single entity. Use the Right click > Split Stack command to slide a specific via of the stack.



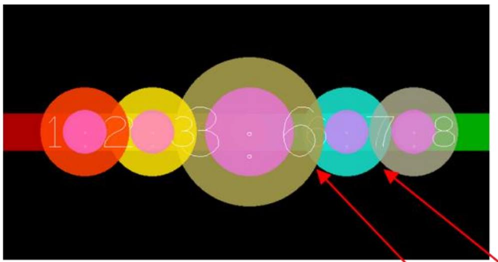
Objects			
Type	S	Name	
*	*	*	
Dsn		module4_addvia	
PCS		DEFAULT	
PCS		OVERLAP	
PCS		STACKED_UVIAS_ONLY	
PCS		STACK_ALL	
LTyp		Conductor	
Lyr	1	TOP	
Lyr	2	SIGNAL_2	
Lyr	3	SIGNAL_3	
Lyr	4	SIGNAL_4	
Lyr	5	SIGNAL_5	
Lyr	6	SIGNAL_6	
Lyr	7	SIGNAL_7	
Lyr	8	BOTTOM	

Vias	BB Via Stagger		Allow
	Min	Max	Pad-Pad Connect
	mm	mm	
*	*	*	*
BB1-2:BB2-3:BB-CORE3-6:B...	0.0000	0.5080	VIAS_PINS_ONLY
BB1-2:BB2-3:BB-CORE3-6:B...	0.0000	0.5080	VIAS_PINS_ONLY
BB1-2:BB2-3:BB-CORE3-6:B...	0.0000	0.5080	VIAS_PINS_ONLY...
BB1-2:BB2-3:BB-CORE3-6:B...	0.0000	0.5080	VIAS_PINS_ONLY...
BB1-2:BB2-3:BB-CORE3-6:B...	0.0000	0.5080	VIAS_PINS_ONLY...
	0.0000	20.0000	VIAS_VIAS_ONLY
	0.0000	0.5080	VIAS_PINS_ONLY
	0.0000	0.5080	VIAS_VIAS_ONLY
	0.0000	0.5080	VIAS_VIAS_ONLY
	0.0000	0.5080	VIAS_VIAS_ONLY
	0.0000	0.5080	VIAS_VIAS_ONLY
	0.0000	0.5080	VIAS_VIAS_ONLY
	0.0000	0.5080	VIAS_PINS_ONLY

Example 4 – Adding Inset Vias

The following vias are used in sequence (BB1-2, BB2-3, BB3-6, BB6-7, BB7-8) however in this example, rules permit the overlapping of adjacent vias.

- While routing on Layer Top (1), a Left double-click produces the Via Popup GUI where Layer Bottom (8) is selected.
- BB1-2 is inserted at the pick location; BB2-3 floating on cursor overlapping BB1-2.
- Separation of vias is controlled by the Same Net rule of -1 between via types in combination of Via to Hole rule set to 0. It's the Via to Hole rule that controls the separation between the edge of the via pad and edge of hole.
- The Via to Hole constraint of 0 allows the tangent condition between the vias (pad edge to hole edge)
- The -1 entry bypasses the same net check in favour of the Via to Hole check. If not for the -1 entry, a same net v-v DRC would be produced by the overlap.
- Remaining vias are added sequentially



Same Net Spacing
- Same Net Spacing Constraint Set
  - All Layers
- Net
  - All Layers
- Region
  - All Layers

Objects			Microvia To										
Type	S	Name	All	Line	Thru Pin	SMD Pin	Test Pin	Thru Via	BB Via	Test Via	Microvia	Shape	Bond Finger
			mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm
*	*	*	*	*	*	*	*	*	*	*	*	*	*
Dsn		module4_addvia	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270
SNSC		DEFAULT	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270	0.1270
SNSC		OVERLAP	***	0.1270	0.1270	0.1270	0.1270	0.1270	-1.0000	0.1270	-1.0000	0.1270	0.1270
LTyp		Conductor	***	0.1270	0.1270	0.1270	0.1270	0.1270	-1.0000	0.1270	-1.0000	0.1270	0.1270
Lyr	1	TOP	***	0.1270	0.1270	0.1270	0.1270	0.1270	-1.0000	0.1270	-1.0000	0.1270	0.1270
Lyr	2	SIGNAL_2	***	0.1270	0.1270	0.1270	0.1270	0.1270	-1.0000	0.1270	-1.0000	0.1270	0.1270
Lyr	3	SIGNAL_3	***	0.1270	0.1270	0.1270	0.1270	0.1270	-1.0000	0.1270	-1.0000	0.1270	0.1270
Lyr	4	SIGNAL_4	***	0.1270	0.1270	0.1270	0.1270	0.1270	-1.0000	0.1270	-1.0000	0.1270	0.1270
Lyr	5	SIGNAL_5	***	0.1270	0.1270	0.1270	0.1270	0.1270	-1.0000	0.1270	-1.0000	0.1270	0.1270
Lyr	6	SIGNAL_6	***	0.1270	0.1270	0.1270	0.1270	0.1270	-1.0000	0.1270	-1.0000	0.1270	0.1270
Lyr	7	SIGNAL_7	***	0.1270	0.1270	0.1270	0.1270	0.1270	-1.0000	0.1270	-1.0000	0.1270	0.1270
Lyr	8	BOTTOM	***	0.1270	0.1270	0.1270	0.1270	0.1270	-1.0000	0.1270	-1.0000	0.1270	0.1270

Example 5 – Adding "Any layer Vias"

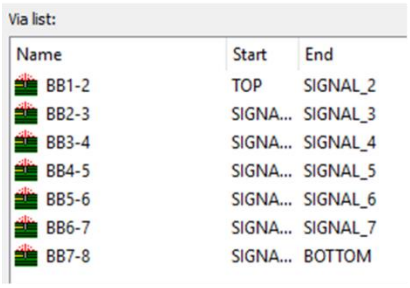
The lamination of conductive areas on each layer to conductive areas on the adjacent layers is commonly referred to as "Any Layer Via" construction. Companies providing this technology include ALIVH from Matsushita and FVSS from Ibiden. This technology is primarily used on small consumer electronic products like cell phones to meet high density routing and board thickness requirements.

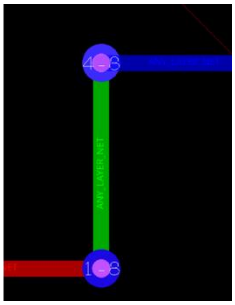
The following vias are used to transition to any layer (BB1-2, BB2-3, BB3-4, BB4-5, BB6-7, BB7-8).

- While routing on Layer Top (1), a Left double-click produces the Via Popup GUI where Layer Bottom (8) is selected.
- The entire range of vias is inserted at the pick point.
- From the Bottom layer, a Left double-click to Signal_4 is made; the entire stack between this span is added. The via label is indicative of the complete stacked series of vias (4-8)
- Physical CSet rules to allow stacking include:

- Min BB Stagger set to 0
- Allow Pad to Pad Connect set to Vias_Vias_only on all layers except Top and Bottom where settings support Via-in-Pad.

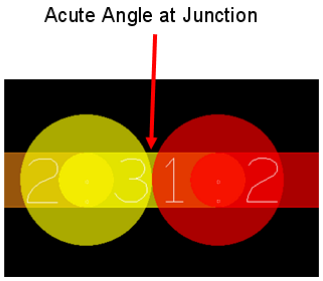
- The slide command treats the stacked vias as a single entity. Use the Right click > Split Stack command to slide a specific via of the stack.





Line Fattening between Tangent Vias

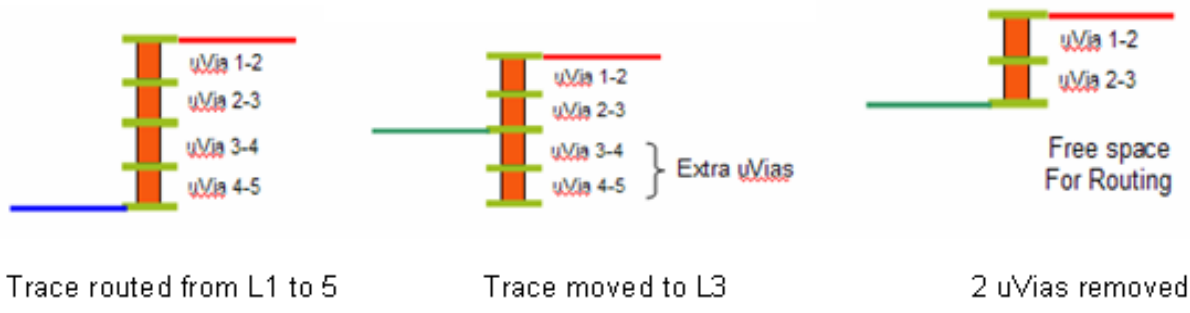
A post route task associated with HDI Design involves increasing the line width between two tangent vias. This is done to remove the acute angle formation between at the junction of the vias.



A post route utility is available to fatten lines between vias based on a user defined edge to edge clearance. The algorithm determined the line width based on the smaller of the two vias. Options are available to 'waive' impedance or max line width DRCs that may result. Users are advised to run this utility near the end of the design process as it's not possible to perform a reset of line width. Use Route > Resize/Respace > Via-Via Line fattening.

Elimination of Unused B/B Vias in Stack

Often vias in a stack may become orphaned as a result of changes made during routing or clip-boarding. The end result leaves unwanted vias that occupy valuable routing real-estate and also contribute to stub effects on the signal.



Unused B/B Via Report

This report detects unused Buried or Blind vias included in a stack. The removal of these vias can open up routing real estate and reduce stub effects at the via site.

The report is located in Tools > Reports (Allegro) or Export > Reports (OrCAD) and is called Unused Blind/Buried Via Report.

Dynamic Pad Suppression

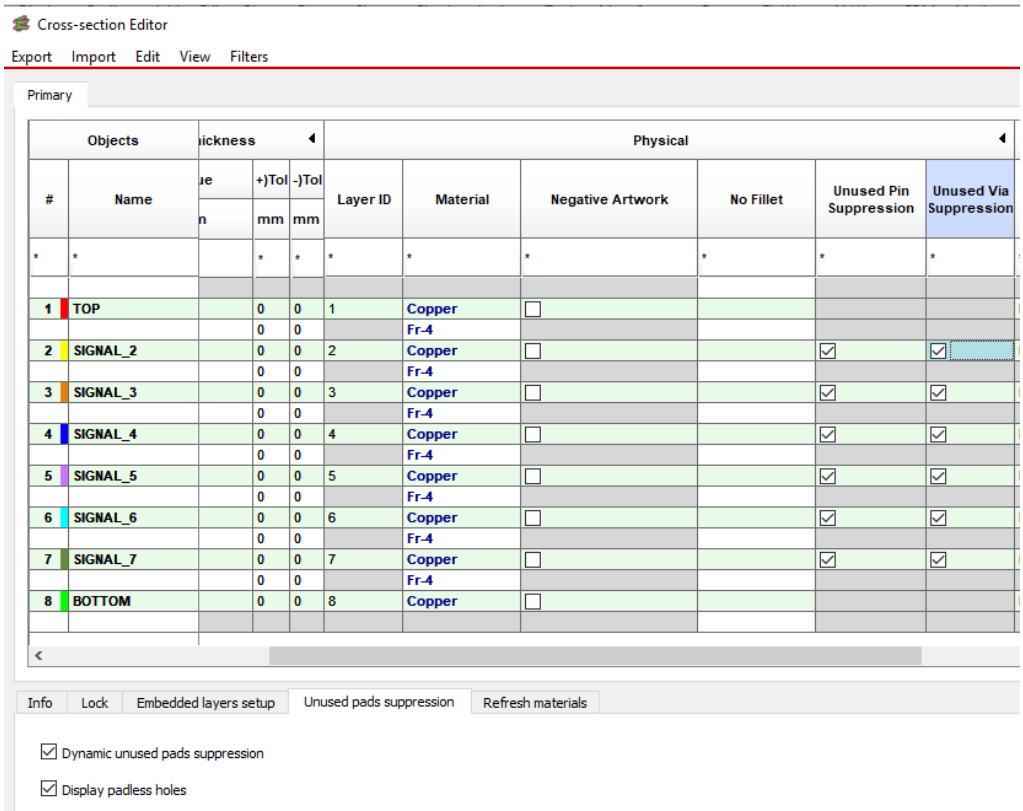
Dynamic Unused Inner Layer Pad Suppression moves what has been historically a post processing application to reduce capacitance effects at each hole site into the design database. Typically, the fabricator's CAM department handled this application prior to film generation, and possibly the OEM removed the pads as a function of artwork generation. With the ever-increasing demand to make product smaller, lighter and cheaper, unused inner layer pads are being removed not only for electrical but also for physical effects. Removing pads increases higher routing densities by allowing traces to be closer to the hole edge. High-temperature, lead-free soldering requires that pads be left on unconnected thru pins, but not on unconnected vias. This application is not only object-based (pin versus via), but also layer based to retain the pads on thru pins on the signal layers closest to the surface layers.

User Interface

Unused Pads Suppression is available by choosing Setup > Cross Section. Each layer of the stack-up is represented. Settings for pins and vias can be enabled on a per- layer basis. Double click the Physical Header to expand the section. Enabling the Dynamic Unused Pads Suppression option automatically enables the display of padless holes.

Layer Restrictions

Layers not available for pad suppression include the Top and Bottom Layers, Negative planes and the begin/end layers of a B/B via. The UI will display outer and plane layers for reference only.



Other Restrictions

Pads associated with Mechanical Pins are not eligible for removal.

Dynamic Suppression

Pad suppression becomes dynamic once the Dynamic Unused Pad Suppression option is enabled, and the dialog box closes. Suppression or restoration occurs on the fly. Upon closing the form, all eligible pads are suppressed. Pads are restored as connections are made to pins or vias. In contrast, pads are dynamically suppressed if traces are deleted from pins or vias. Disabling the dynamic option restores all pads on pins and vias. DRCs may result if traces become closer to the drill hole. The pad definition remains unchanged as a result of suppression.

Exception Properties

The UNUSED_PADS_IGNORE property prevents pad suppression at the symbol, net, pin, or via level. Once applied, pads remain static on the respective elements. The UNUSED_PADS_OVERRIDE property allows pads to be removed on outer layers. The property is restricted to a symbol with values of Top, Bottom, or Top:Bottom. Consider using on edge connectors to minimize the amount of gold used during plating.

Artwork Alignment

When Dynamic Unused Pads Suppression is enabled, the legacy film control Suppress Unconnected Pads option and functionality appears enabled for all films but greyed out and non-editable: Database-driven suppression occurs. If dynamic suppression is not enabled; however, the checkboxes are individually editable as needed, and legacy suppression occurs instead. Legacy suppression handles blind and buried vias where the begin and end layer pads must never be suppressed, even if unconnected and on an internal layer.

Router Interface

Full pad definitions pass to the Allegro PCB Router, which cause DRCs within the router application.

Drill to Metal DRC

Drill hole to metal-based checking covers both holes associated with circuitry (pins and vias) and holes associated with mechanical pins, where the antipad can be used as an implicit route keepout area.

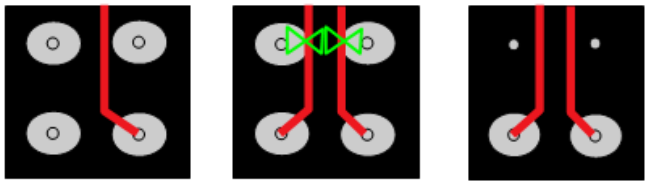
Drill holes are commonly referred by their plating category; plated or non-plated. The suite of drill hole checks are based on Allegro PCB Editor pin types (connect and mechanical pins). Typically connect-pin-based holes are plated; mechanical-pin-based holes, non-plated. It is possible, however, to define each type as plated or non-plated. Logic can only be assigned to a connect pin.

The term hole is used in the DRC system and Constraint Manager as the drill hole associated with circuit-based pins and vias. Unlike computer-aided-manufacturing checks, where generic PTH to metal checking occurs against minimum constraint values, an integrated CAD system must provide the flexibility to check holes against the diverse set of net-based rules. For example, if the rules for a 60V net to GND via or pin require a 1-mm clearance, this same clearance would be required to the edge of the padless holes associated with these elements.

A hole-to-metal check occurs only when the respective hole is void of pads on conducting layers. This can be a result of Null pad entries in the padstack definition or instance or using the dynamic pad suppression. When pads exist on pins and vias, the hole check yields to the conventional pin and via checks.

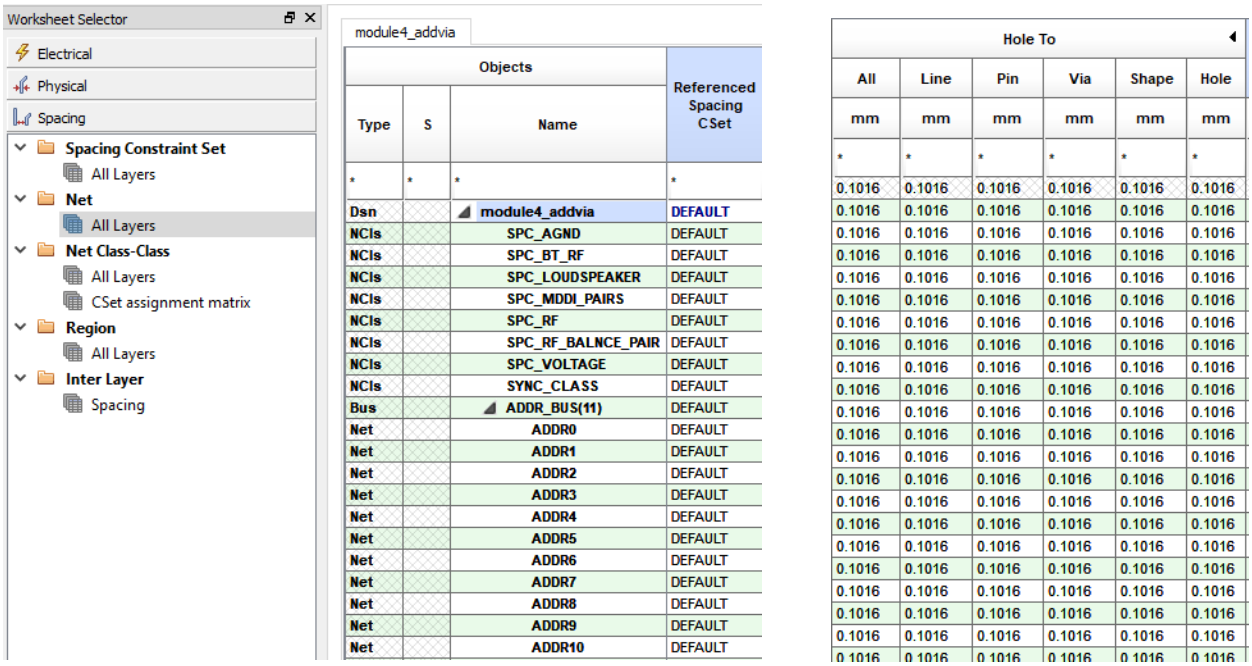
The following example illustrates the potential benefits of drill-based checks. The channel width with pads present restricts the number of lines routed between the pin pads to just one. The removal of used pads, coupled

with a hole-to-line space that permits the line to be routed closer to the hole edge but tangent to the annular ring, opens the channel to permit two lines between.



Constraint Manager Integration

Hole to metal-based constraints can be driven from Spacing CSets or directly set on Net based objects in Constraint Manager. Both the Spacing and Same Net Spacing domains support a suite of Hole to (Line, Pin, Via, Shape and Hole) spacing checks. On new boards, hole-based constraints default to 8 mils; all other spacing constraints default to 5 mils. On uprev'd boards, hole-based constraints are derived from the Spacing CSets to ensure metal to- hole spacing aligns with net-spacing rules. A hole-to-metal DRC occurs when the hole is seen as the outer extent of the pin/via element. If a pad is present and larger than the hole, the spacing DRC heck geometry against the pad extents. Both a hole and a pin/via pad violation cannot occur on the same element.

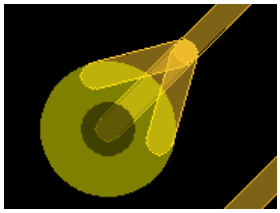


Dynamic Filleting

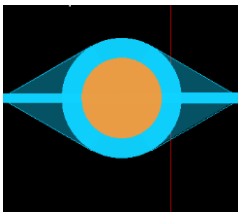
The gloss-based fillet application updates fillets dynamically on pins, vias, or T-junctions. The application continues to support interactive or batch mode as well as existing parameters. The Dynamic Fillets option on the Pad and T Connection Fillet dialog box offers the convenience of filleting during interactive etch editing with no additional procedures. When this option is enabled (Allegro PCB Designer only), fillets are added when a connection is made to an element or deleted when removed.

Shape-based Fill

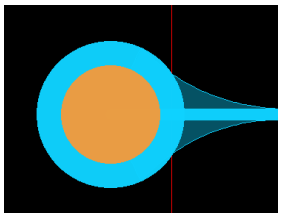
The fill associated with fillets has transitioned from line to shape-based. A single entity fillet is managed more efficiently in the database. For DRC considerations, the fillet should be regarded as an extension of the pin or via.



Line-based Fillet



Shape-based Straight Fillet



Shape-based Curved Fillet

Parameters

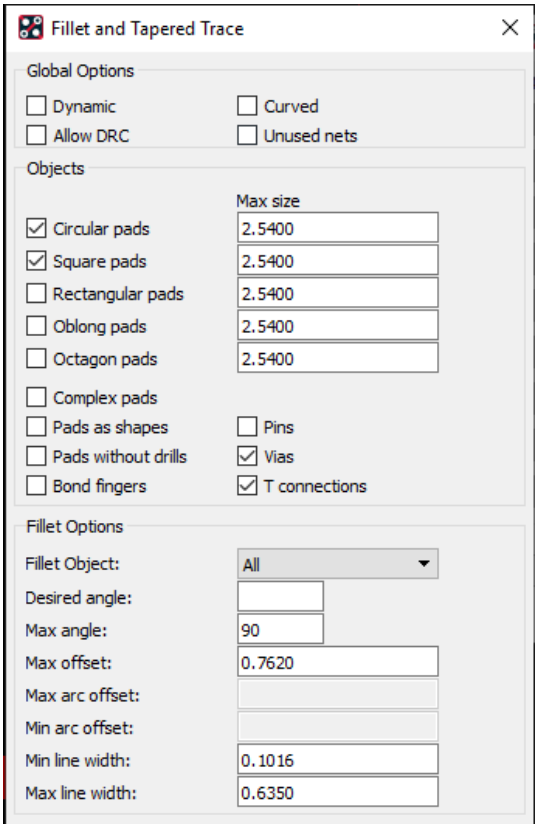
Parameters associated with the fillet application include:

Dynamic - Updates the entire board with shape-based fillets. During subsequent interactive route editing, fillets are deleted and then regenerated on modified pins or vias, based on the specified parameters (unless an element has the NO_FILLET property assigned). If disabled, shape-based fillets are added in a batch update. Whenever you modify a pin, via, or cline, the tool deletes the fillets and does not regenerate them.

Curved - Creates shape-based fillets or tapered traces using an arc instead of a line as part of the shape outline from the cline to the pad intersection.

Allow DRC - Creates fillets and taper traces even if DRCs result.

Unused Nets - Allows tapering and filleting on unused nets.



Objects - Choose options for the pad shapes: circular pads, square pads, rectangular pads, oblong pads, octagon pads, pads as shapes, pins, vias, bond fingers, pads without drills, and t connections. For circular, square, rectangular, octagon and oblong pads, you can indicate the maximum size for the fillet. The default size is 2.54mm (in drawing units).

Fillet Objects - Specifies the object for fillet. Valid objects are Pins, Vias and Ts.

Desired angle - Specifies the angle created by the generated fillet shapes. The default value is 90 degrees. A larger Desired Angle and a smaller Max Offset create a short fillet. A smaller Desired Angle and larger Max Offset create a long fillet. This option is not applicable for creating arc fillets.

Max angle - Specifies the maximum angle for the fillet. The default value is 90 degrees. The maximum possible value is 99 degrees. This value must always be equal to or greater than the Desired Angle. A larger Desired Angle and a smaller Max Offset create a short fillet. A smaller Desired Angle and larger Max Offset create a long fillet. This option is not applicable for creating arc fillets.

Max offset - Specifies the maximum distance between the intersection of the pad edge and the connecting line, forming the fillet length. The default value is 0.635mm (in drawing units). This option is not applicable for creating arc fillets.

Max arc offset - Specifies the maximum distance between the pad edge and the point along the curved trace, forming the fillet length. The default value is 0.127mm (in drawing units).

Min arc offset - Specifies the minimum distance between the pad edge and the point along the curved trace, forming the fillet length. The default value is 0.0254mm (in drawing units). Must always be lesser than the Max arc offset. You can fillet arc segments for only pins and vias. The fillets generated for arc segments always have curved lines.

Min line width - Specifies the minimum line width of the cline entering the pad. If the line width of the cline is less than the value specified here, the fillet is not created. The default value is 0.0762mm (in drawing units).

Max line width - Specifies the maximum line width of the cline entering the pad. If the line width of the cline is greater than the value specified here, the fillet is not created. The default value is 0.635mm (in drawing units).

Fillet Algorithm

The algorithm first tries to create the fillet at the desired angle, tangent to the pad. If the fillet cannot be created, the angle increments to the Max Angle. If the fillet length, pad tip to vertex of fillet, is greater than the Max Offset, the vertex is adjusted by an amount to satisfy the Max Offset requirement. The end points of the fillet are adjusted by the same amount to maintain the angle.

Reporting

The Missing Fillets Report lists junctions with missing or partial fillets and is accessed with Tools > Reports or Tools > Quick Reports (Allegro) or Export > Reports or Export > Quick Reports (OrCAD)..