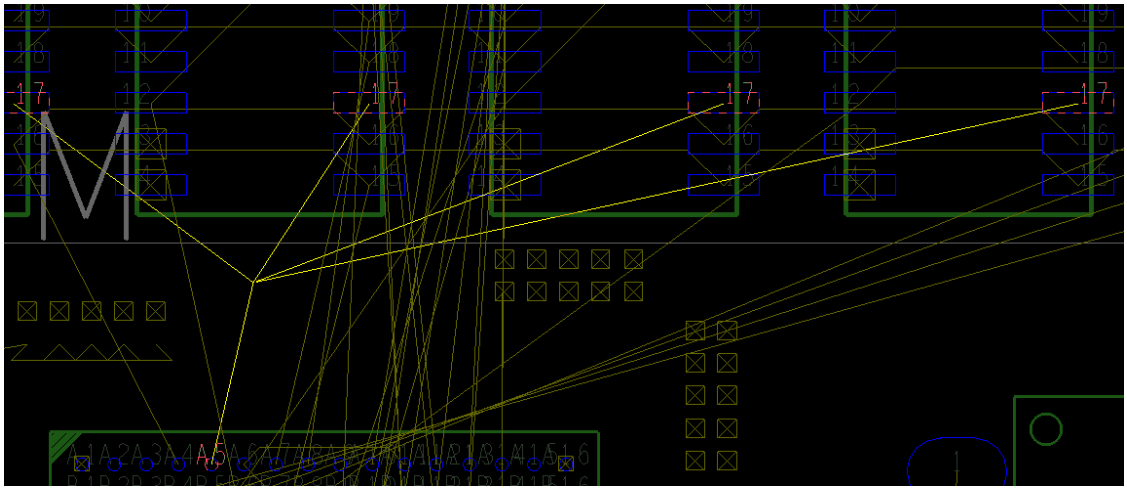
Introduction

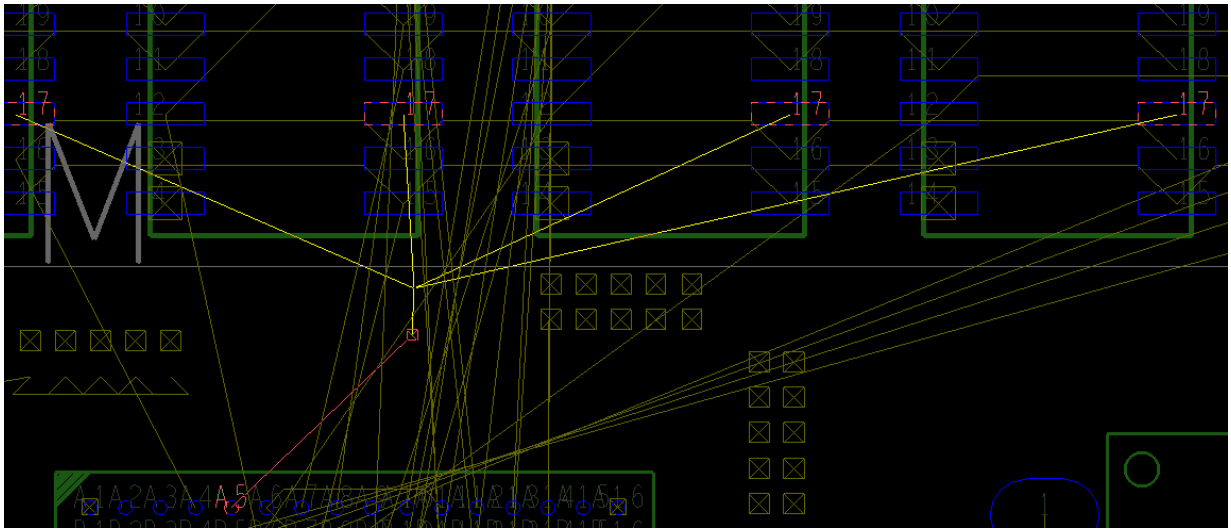
Many designs today require nets to be routed in a particular way. Take the example of a processor feeding four memory devices, the signal from the processor (driver) MUST arrive at the memory devices (receivers) at exactly the same time. To achieve this Cadence PCB tools offer several options to schedule the net, then the ability to match the length of track from a virtual point (T-Point) to the (x) number of receivers. This is license dependent.

Net Scheduling

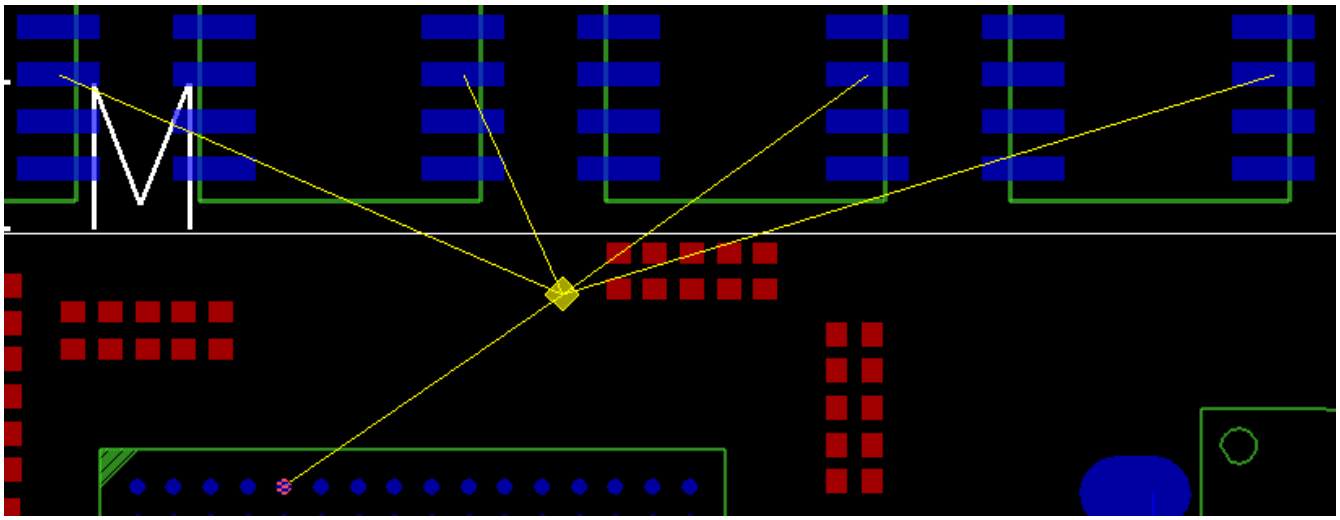
You must use an OrCAD PCB Designer Professional or an Allegro PCB Designer license level or higher to be able to run this function. To start, locate the net that you want to schedule and use Logic > Net Schedule (Allegro) or Edit > Net Schedule (OrCAD). Then with a left click select the required net. The whole net highlights and is displayed as a starpoint as shown below:-



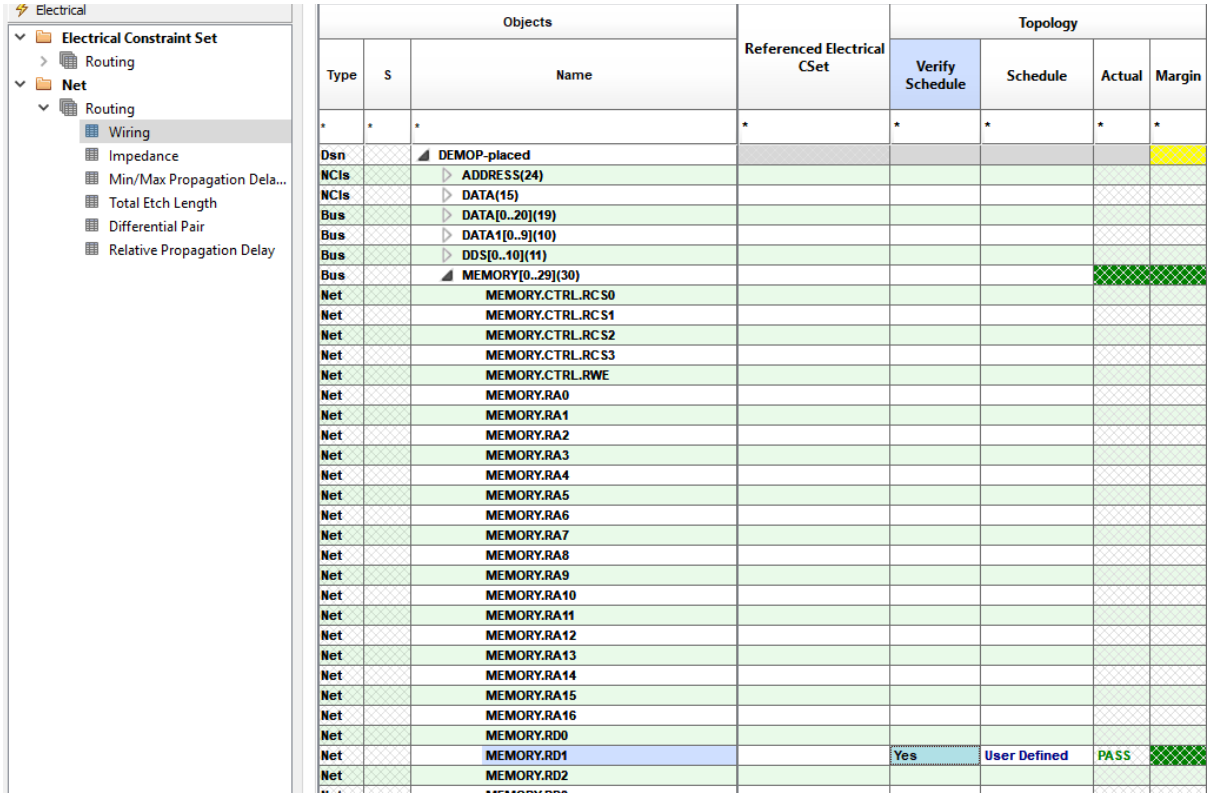
The command line prompts pick to select pin/rat-T on net “netname”. For this example the pin on the processor is selected first with a left click. The next selection required is to insert a virtual point (T-point) which is a location on the board that all the other locations of the net will start from. Use right click > Insert T, and then with the left click select the T Point location. A marker is displayed at this point as shown below.



You are then prompted to pick another point on the net, for this example I will pick pin 17 of the first memory device, then pick the T-Point again, and then the next memory device, then the T-point until the four memory devices and the processor are individually connected via the T-Point. Then use right click > Done to end the command. The net will now be displayed as shown below with the T Point displayed as a diamond. This is effectively a user defined schedule. You can create any schedule you require using this method but this method always creates a user defined schedule which will be displayed in Constraint Manager.

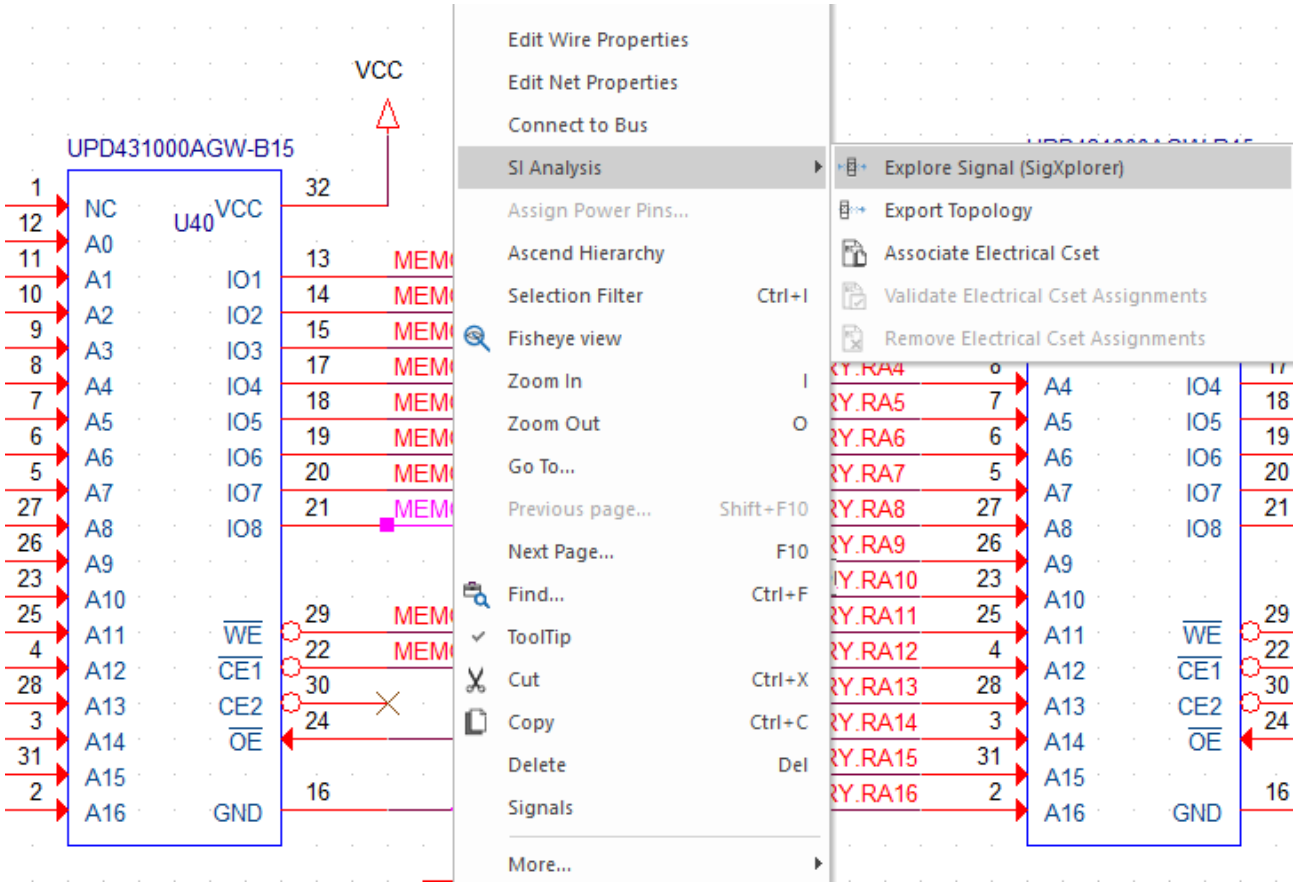


Once the schedule has been defined you can ensure that the routed tracks meet this schedule. There is a setting in Constraint Manager to verify any schedule that has been applied. In Constraint Manager > Electrical > Net > Wiring worksheet, locate the net. There is a **UserDefined** setting in the schedule column. To ensure the routing meets this schedule, select the Verify Schedule column and define a “Yes”. This will DRC the net should your routing not match the schedule defined.

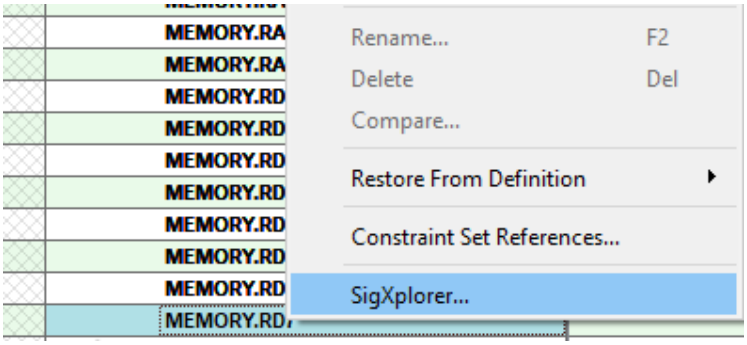


Objects			Referenced Electrical CSet	Topology			
Type	S	Name		Verify Schedule	Schedule	Actual	Margin
*	*	*	*	*	*	*	*
Dsn		DEMOP-placed					
NCls		ADDRESS(24)					
NCls		DATA(15)					
Bus		DATA[0..20](19)					
Bus		DATA1[0..9](10)					
Bus		DDS[0..10](11)					
Bus		MEMORY[0..29](30)					
Net		MEMORY.CTRL.RCS0					
Net		MEMORY.CTRL.RCS1					
Net		MEMORY.CTRL.RCS2					
Net		MEMORY.CTRL.RCS3					
Net		MEMORY.CTRL.RWE					
Net		MEMORY.RA0					
Net		MEMORY.RA1					
Net		MEMORY.RA2					
Net		MEMORY.RA3					
Net		MEMORY.RA4					
Net		MEMORY.RA5					
Net		MEMORY.RA6					
Net		MEMORY.RA7					
Net		MEMORY.RA8					
Net		MEMORY.RA9					
Net		MEMORY.RA10					
Net		MEMORY.RA11					
Net		MEMORY.RA12					
Net		MEMORY.RA13					
Net		MEMORY.RA14					
Net		MEMORY.RA15					
Net		MEMORY.RA16					
Net		MEMORY.RD0					
Net		MEMORY.RD1		Yes	User Defined	PASS	
Net		MEMORY.RD2					

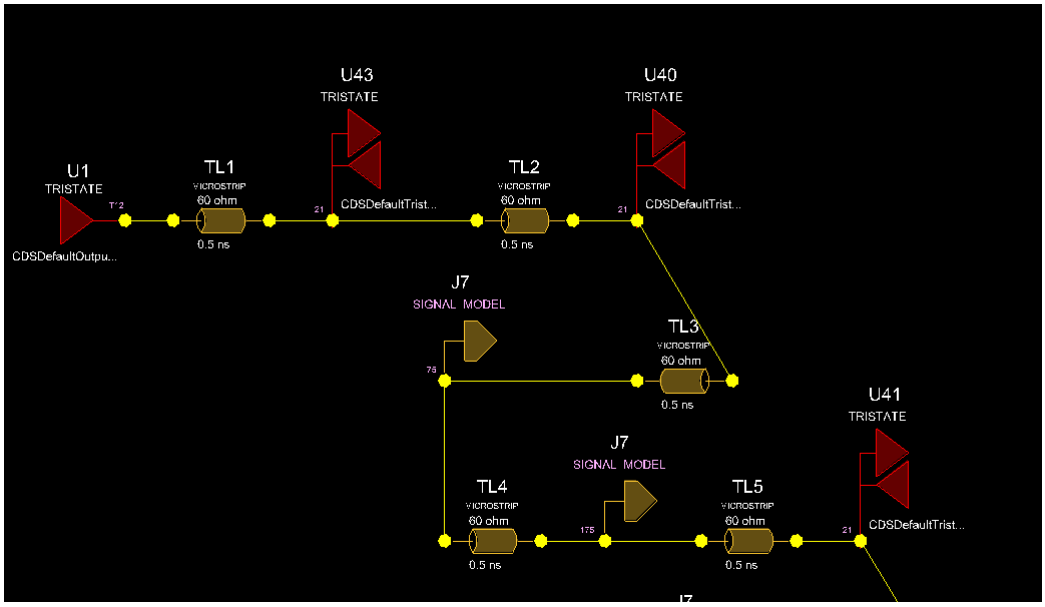
You can also define the schedule by using Signal Explorer which is available from most licenses in the Cadence front and back end tools. The methods to get the schedule into PCB Editor are license dependant though. If you are using OrCAD Capture (Capture CIS) you can select the net on the canvas and choose right click > SI Analysis > Explore Signal (SigXplorer) which will launch the Signal Explorer tools.



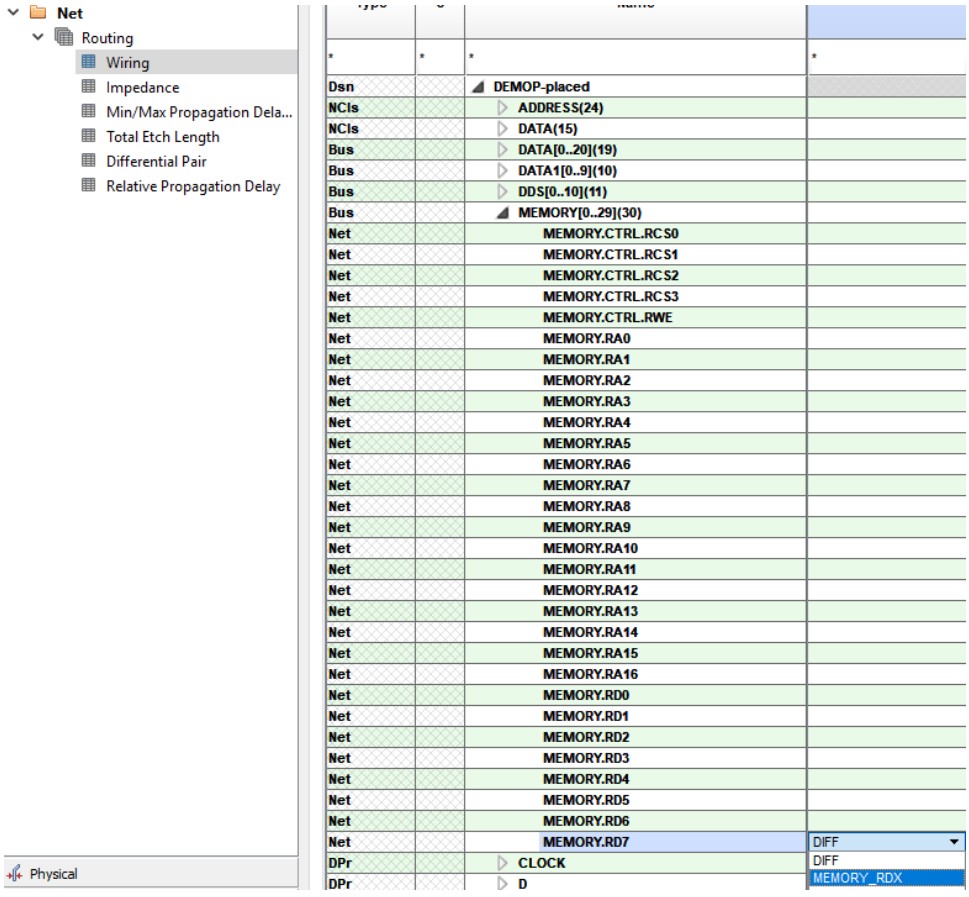
Note this procedure only works if the schematic is NOT Constraint Manager enabled. If it is then you can select the net from within Constraint Manager and right click > SigXplorer.



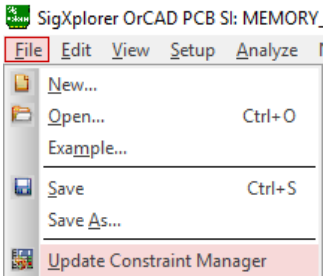
Once the tools launch you can adjust the schedule to match your requirements. This can be done by deleting the existing wiring (left click on the wire). To add new wiring left click on a pin of a device, left click on another pin to make the connection.



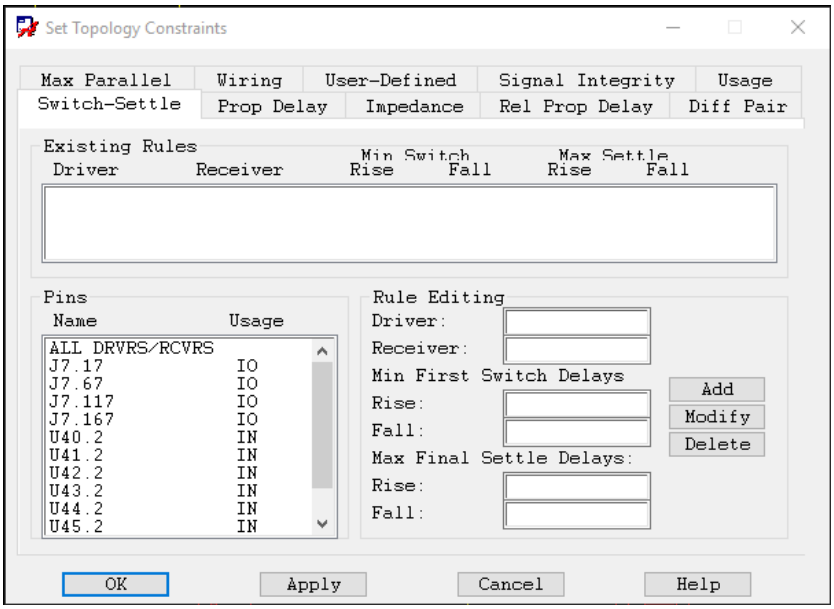
Once complete use the File > Save which writes a Topology file (filename.top). This can be imported from within Constraint Manager using File > Import > Electrical CSet. This can then be applied to the relevant net(s) by choosing the Imported Referenced Electrical CSet rule from the Net > Routing > Wiring worksheet as shown below. This would then be applied as a Template based schedule which can also be verified.



Net	MEMORY.RD0	RDX	Yes	TEMPLATE	PASS
Net	MEMORY.RD1	RDX	Yes	TEMPLATE	PASS
Net	MEMORY.RD2	RDX	Yes	TEMPLATE	PASS
Net	MEMORY.RD3	RDX	Yes	TEMPLATE	PASS
Net	MEMORY.RD4	RDX	Yes	TEMPLATE	PASS
Net	MEMORY.RD5	RDX	Yes	TEMPLATE	PASS
Net	MEMORY.RD6	RDX	Yes	TEMPLATE	PASS
Net	MEMORY.RD7	RDX	Yes	TEMPLATE	PASS

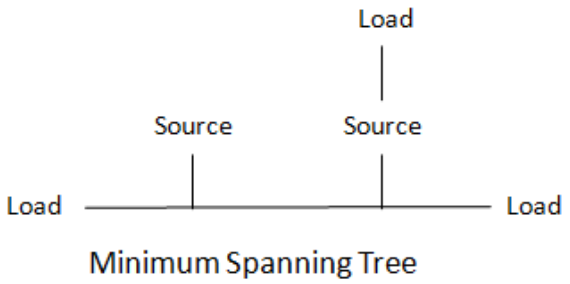


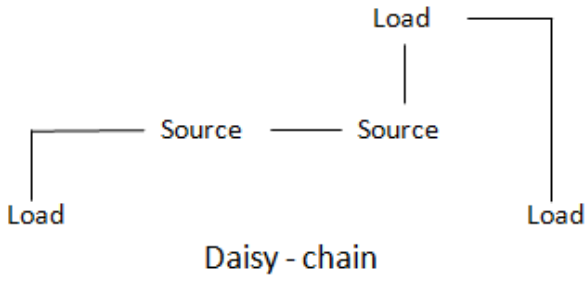
If you have access to Allegro PCB Designer + High Speed License or OrCAD PCB SI or any of the Sigrity based licenses you can repeat the process of selecting the net and launching Signal Explorer but once you have completed the scheduling of the net you can choose File > Update Constraint Manager which will write any changes you make in Signal Explorer directly into Constraint Manager.
You also have the ability to set other Electrical based rules using the Setup > Constraints option which are also saved back to Constraint Manager using this method.

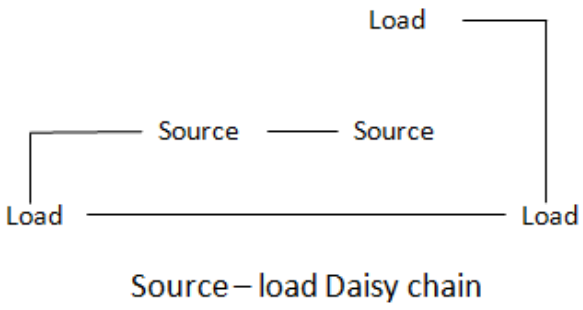


Another pre-set way to schedule the pins in a net is to select from a list of defined schedules shown below. The PCB Editor applies the selected schedule to the net(s) based on part placement and pin type. The selection list is available from the schedule column in Constraint Manager > Wiring. There are five types: -

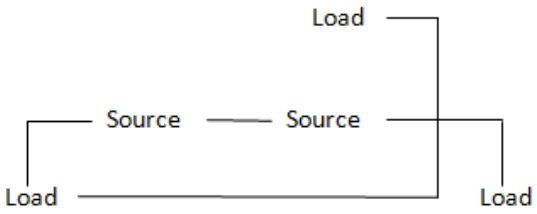
Minimum Spanning Tree connects all pins together for minimum length.
Daisy Chain connects all pins in a point-to-point sequence. Each pin connects to a maximum of two other pins (pin type is still not observed).
Source Load Daisy Chain is similar to a simple daisy chain, except that all drivers are sequenced first, and followed by all receiver pins.
Far End Cluster is similar to a star schedule except that the last driver pin connects to a T point to which all of the receivers are connected.
Star schedules the driver pins in a daisy chain fashion and then all of the receiver pins are individually connected to the last driver pin.







Source – load Daisy chain

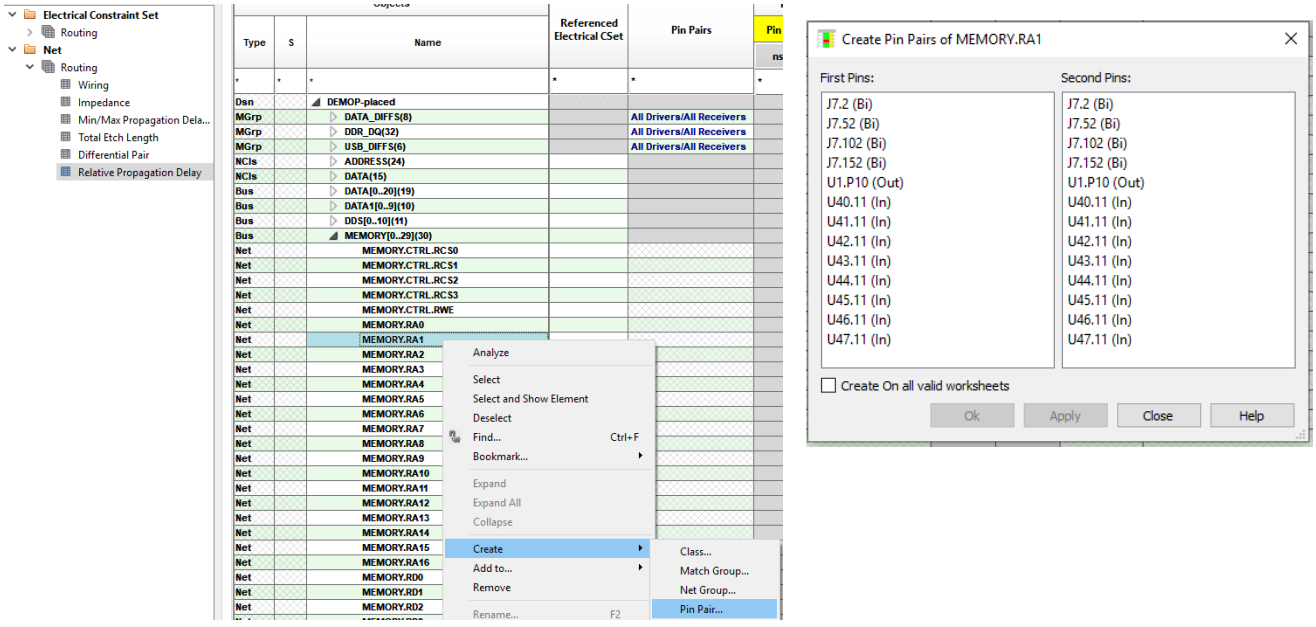


Far – end Cluster

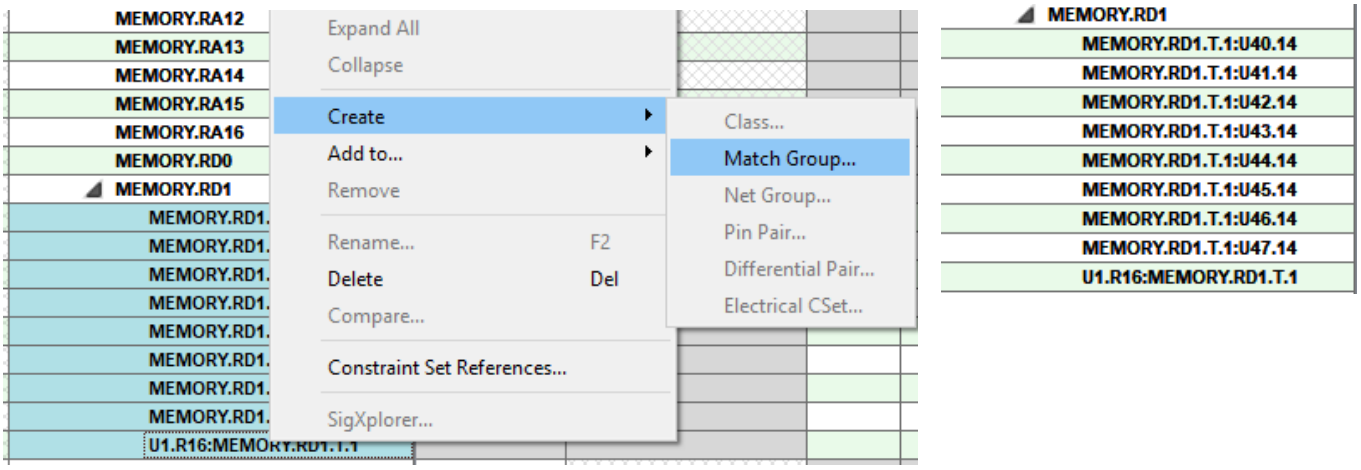
Other Wiring Parameters:

The Mapping Mode field (Electrical Constraint Set > Routing > Wiring)- is used when you assign an ECSet to a net, Xnet, or bus. This setting controls how the driver(s) and receiver(s) within the ECSet are matched to their corresponding pins within the net. The options include Pinuse, Refdes, or Pinuse and Refdes. Note Mapping mode along with Exposed Length and Parallel are only available with the Allegro PCB Designer license.

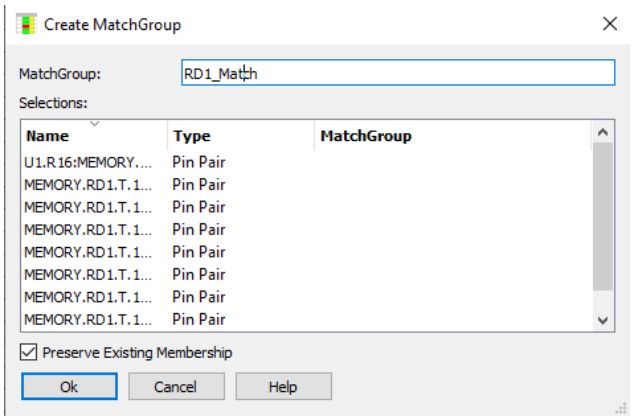
Stub Length rule controls the length of branches off the transmission line.
Exposed Length rule controls the amount of surface layer routing allowed on nets that you prefer to route inside when these nets need to tie to a surface-mount pin.
Parallel rule lets you specify how long a signal can run parallel to another signal, and at what spacing (edge to edge). You can define up to four length/distance pairs. Although the PCB Router implements this rule on a segment basis, the PCB Editor DRC is cumulative.
Layer Sets allow you to define the specific layers used for a Netclass or net.
The next step is to split the nets into individual pin pairs (for example point1 to point2). This operation is completed in the Constraint Manager > Electrical > Net > Relative Propagation Delay worksheet. Select the net in question and then right click > Create > Pin Pairs



The pin pair GUI will appear and allow you to create a multiple group of point to point connections for the specific net. If you want to create different physical rules for the pin pairs ensure that the “Create on all valid worksheets” is checked so that the pin pairs can have physical rules applied to them.



We now want to create a matched group of the 4 pin pairs from the T-Point to the memory devices. This gives you the ability to set an equal length rule so that the signals will arrive at the receivers at exactly the same time. To define these use Shift + left click and select the relevant pin pairs then right click > Create > Match Group. Specify a name and click OK. The Matched Group is added to the top section of Constraint Manager. The pin pairs remain in case you wish to define other rules for these pin pairs.



We now need to set the Matched Group up, define Pin Pairs – Longest Pin Pair, Scope = Global and Delta:tolerance to 0:0.635. Since the nets are not routed, the Actual and Margin cells appear in Yellow. DRC results based on actual unrouted lengths can be produced by setting the DRC Unrouted options for Relative Propagation Delay followed by an update of the DRC system. To enable the DRC from Constraint Manager, go to Analyze > Analysis Modes > Electrical > Electrical Options then enable the “Relative propagation delay” in the DRC unrouted section. The match group will have updated with green and red bars. A Target is automatically assigned to the member of the group with the longest Manhattan length.

Objects			Referenced Electrical CSet	Pin Pairs	Pin Delay		Scope	Relative Delay		
Type	S	Name			Pin 1	Pin 2		Delta:Tolerance	Actual	Margin
					ns	ns		mm		
*	*	*	*	*	*	*	*	*	*	*
Dsn		DEMOG-placed								33.825 mm
MGrp		DATA_DIFFS(8)		All Drivers/All Receivers			Global	0 mm:2.54 mm		
MGrp		DDR_DQ(32)		All Drivers/All Receivers			Global	0 mm:5 mm		
MGrp		RD1_MATCH(9)		Longest Driver/Receiver			Global	0 mm:0.635 mm		33.825 mm
PPr		MEMORY.RD1.T.1:U40.14 [MEMORY.RD1]					Global	0 mm:0.635 mm	1.718 mm	1.083 mm
PPr		MEMORY.RD1.T.1:U41.14 [MEMORY.RD1]					Global	0 mm:0.635 mm	12.632 mm	11.997 mm
PPr		MEMORY.RD1.T.1:U42.14 [MEMORY.RD1]					Global	0 mm:0.635 mm	23.546 mm	22.911 mm
PPr		MEMORY.RD1.T.1:U43.14 [MEMORY.RD1]					Global	0 mm:0.635 mm	34.46 mm	33.825 mm
PPr		MEMORY.RD1.T.1:U44.14 [MEMORY.RD1]					Global	0 mm:0.635 mm	32.742 mm	32.107 mm
PPr		MEMORY.RD1.T.1:U45.14 [MEMORY.RD1]					Global	0 mm:0.635 mm	21.828 mm	21.193 mm
PPr		MEMORY.RD1.T.1:U46.14 [MEMORY.RD1]					Global	0 mm:0.635 mm	10.914 mm	10.279 mm
PPr		MEMORY.RD1.T.1:U47.14 [MEMORY.RD1]					Global	0 mm:0.635 mm	TARGET	
PPr		U1.R16:MEMORY.RD1.T.1 [MEMORY.RD1]					Global	0 mm:0.635 mm	12.519 mm	11.884 mm

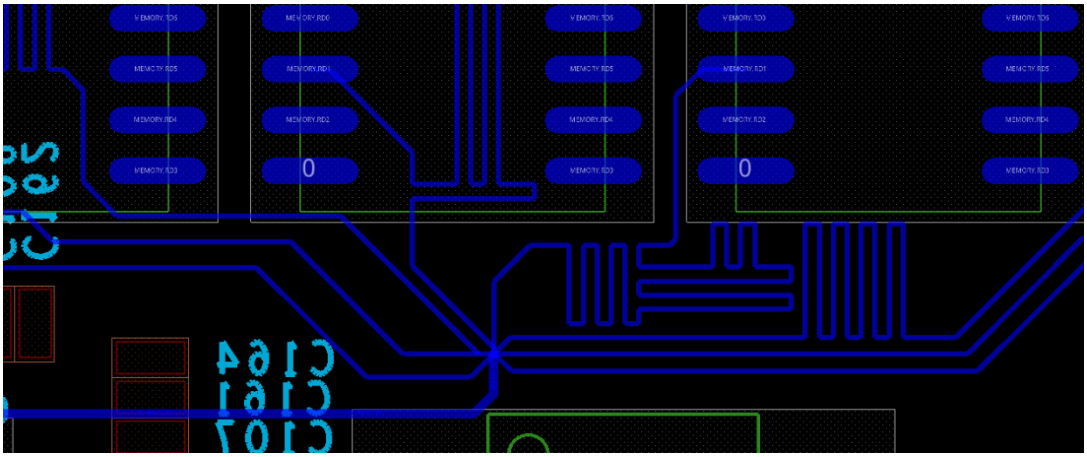
The final option is to define a different physical rule to the “branch” and “trunk” of the net. In some situations you may need to define a thicker track width to the trunk part (Driver – Tpoint) and a thinner track width for the branches (Tpoint – Receiver). Use the Physical domain - Physical Constraints > All Layers and define two new rules one called RD_TRUNK and RD_BRANCH. You can adjust the Min Line Width to suit your requirements.

Objects			Referenced Physical CSet	Line Width	
Type	S	Name		Min	Max
				mm	mm
*	*	*	*	*	*
Dsn		DEMOG-placed	DEFAULT	0.200	0.000
PCS		DEFAULT		0.200	0.000
PCS		RD_BRANCH		0.150	0.000
PCS		RD_TRUNK		0.250	0.000

Once the rules have been defined go to the Net > All Layers workbook in the Physical Domain and Click on the Referenced Physical CSET cell adjacent to the relevant Pin Pair and select apply the RD_TRUNK to one of the Pin Pairs and the RD_BRANCH to the remaining 4 pin pairs.

MEMORY.RD1.T.1:U40.14	RD_BRANCH	0.150
MEMORY.RD1.T.1:U41.14	RD_BRANCH	0.150
MEMORY.RD1.T.1:U42.14	RD_BRANCH	0.150
MEMORY.RD1.T.1:U43.14	RD_BRANCH	0.150
MEMORY.RD1.T.1:U44.14	RD_BRANCH	0.150
MEMORY.RD1.T.1:U45.14	RD_BRANCH	0.150
MEMORY.RD1.T.1:U46.14	RD_BRANCH	0.150
MEMORY.RD1.T.1:U47.14	RD_BRANCH	0.150
U1.R16:MEMORY.RD1.T.1	RD_TRUNK	0.250

You can now go and route the nets and the track thicknesses and lengths will match based on the settings defined in Constraint Manager. You will need to add delay (extra length) to some of the pin pairs to match the lengths. A finished result is shown below.



Constraint Manager View:-

MGrp		RD1_MATCH(9)		Longest Driver/Receiver			Global	0 mm:0.635 mm		0.054 mm
PPr		MEMORY.RD1.T.1:U40.14 [MEMORY.RD1]					Global	0 mm:0.635 mm	0.064 mm	0.571 mm
PPr		MEMORY.RD1.T.1:U41.14 [MEMORY.RD1]					Global	0 mm:0.635 mm	0.581 mm	0.054 mm
PPr		MEMORY.RD1.T.1:U42.14 [MEMORY.RD1]					Global	0 mm:0.635 mm	0.073 mm	0.562 mm
PPr		MEMORY.RD1.T.1:U43.14 [MEMORY.RD1]					Global	0 mm:0.635 mm	0.091 mm	0.544 mm
PPr		MEMORY.RD1.T.1:U44.14 [MEMORY.RD1]					Global	0 mm:0.635 mm	0.46 mm	0.175 mm
PPr		MEMORY.RD1.T.1:U45.14 [MEMORY.RD1]					Global	0 mm:0.635 mm	0.057 mm	0.578 mm
PPr		MEMORY.RD1.T.1:U46.14 [MEMORY.RD1]					Global	0 mm:0.635 mm	0.531 mm	0.104 mm
PPr		MEMORY.RD1.T.1:U47.14 [MEMORY.RD1]					Global	0 mm:0.635 mm	TARGET	
PPr		U1.R16:MEMORY.RD1.T.1 [MEMORY.RD1]					Global	0 mm:0.635 mm	0.017 mm	0.618 mm