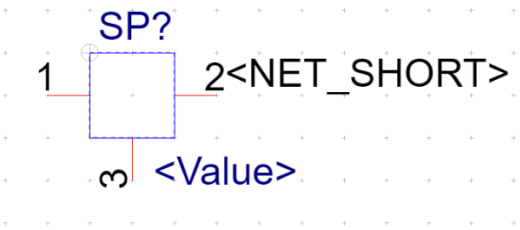
Introduction

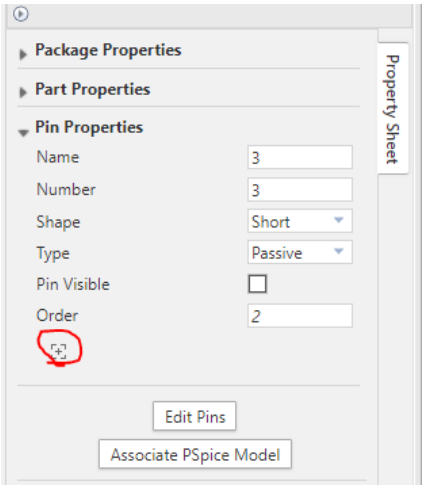
Although PCB Editor will enforce the separation of differently named nets, there is sometimes a requirement to make a common connection between some nets in a design. This is also referred to as a "star point". During normal operation, PCB Editor would report a DRC where these nets were shorted together, this DRC could be waived in PCB Editor, but a better way would be to use the NET_SHORT property. The NET_SHORT property can be assigned to a PIN, VIA or SHAPE and it would be useful to be able to control the net shorting function from the schematic. Since shapes and vias do not exist in the schematic, creating a component symbol and assigning the NET_SHORT property to the component pin, or pins, is the only method available to control the shorting from the schematic. The purpose of the NET_SHORT property is to “allow” the DRC that would be created by the shorted nets. Care **MUST** be taken when using this process.

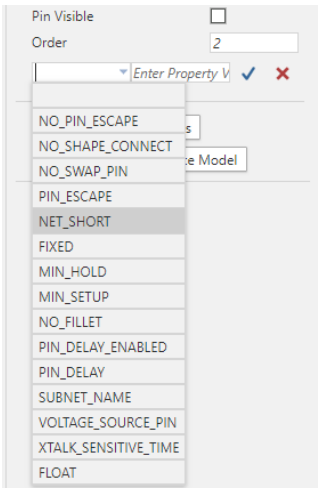
How to make a common connection between two or more nets in PCB Editor

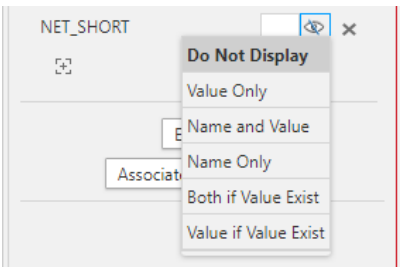
Open OrCAD Capture (OrCAD Capture CIS), open your schematic library then right click > New Part. Then create a new schematic part. The number of pins required relates to the number of nets you wish to short. For this example we are going to short three nets together.



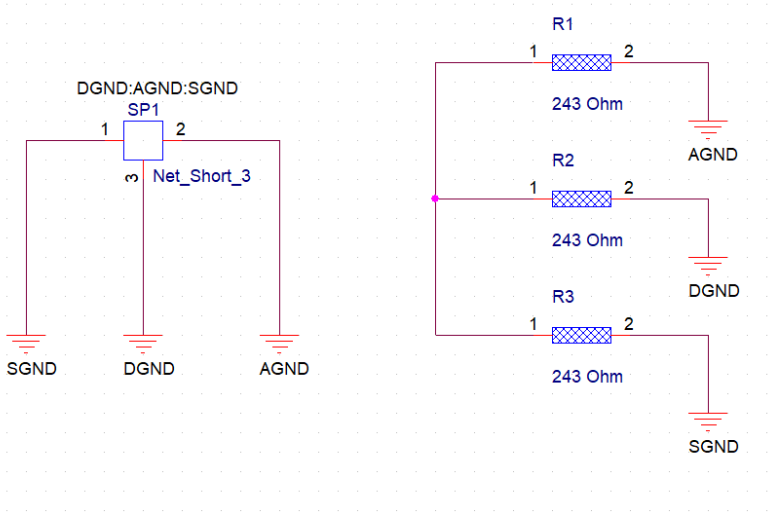
For each pin add a new Pin Property called NET_SHORT with no value. On This example the property is also displayed so it can be viewed in the schematic. To do this select each pin and select the + in the Pin Properties pane (on the right-hand side) then choose NET_SHORT from the property drop-down. Choose the Green Tick to confirm the property. To display the property, select the “eye” icon next to the property and choose Value only.





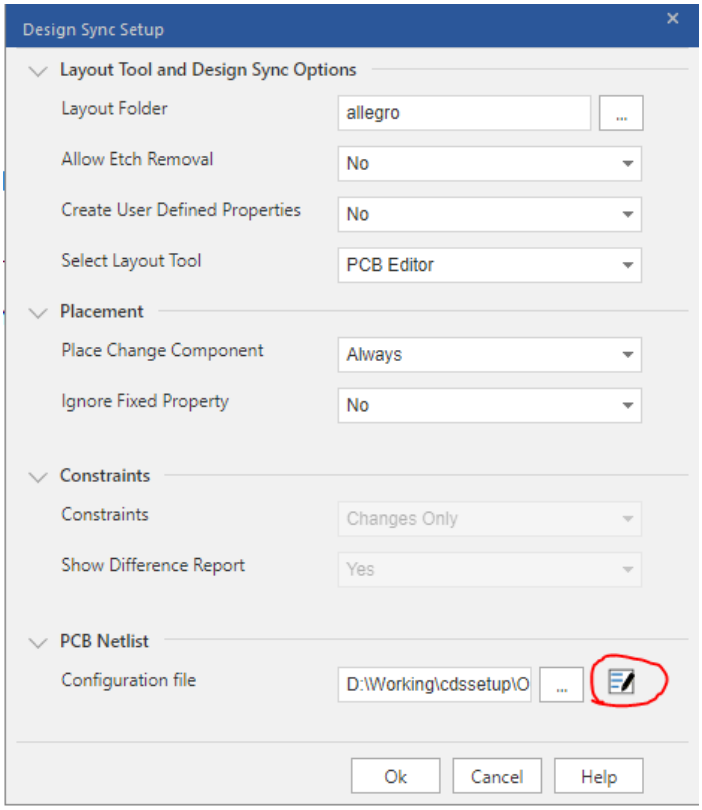


Save the symbol in a default company library. Draw your circuit using the new short symbol to logically define your net short locations on the schematic. An example is shown below.

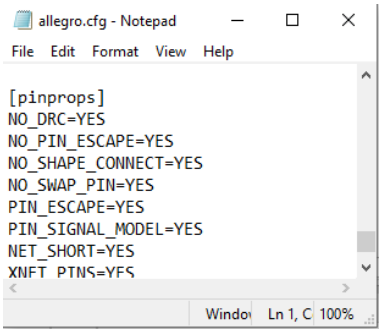


On each pin on the net short (SP1) you will need to Edit Property (Double click the pin) and add the net names that you wish to short separated by a colon. In this example the nets are DGND:AGND:SGND. It is recommended that for each pin the primary net is first (i.e. pin 1 the NET_SHORT would equal SGND:AGND:DGND. You also need to ensure that you also have a PCB footprint defined for the netshort part.

Once your design is complete you will need to run Design sync and create the board file. Before we do this we need to check that the allegro.cfg file contains a pin property to match the NET_SHORT property we defined in the symbol. This is set by default so you only need these steps if you have customized your allegro.cfg file. If required follow these steps to add the property. To do this select the dsn file in the project window and then run PCB > Design Sync Setup. Click to edit the Configuration file.

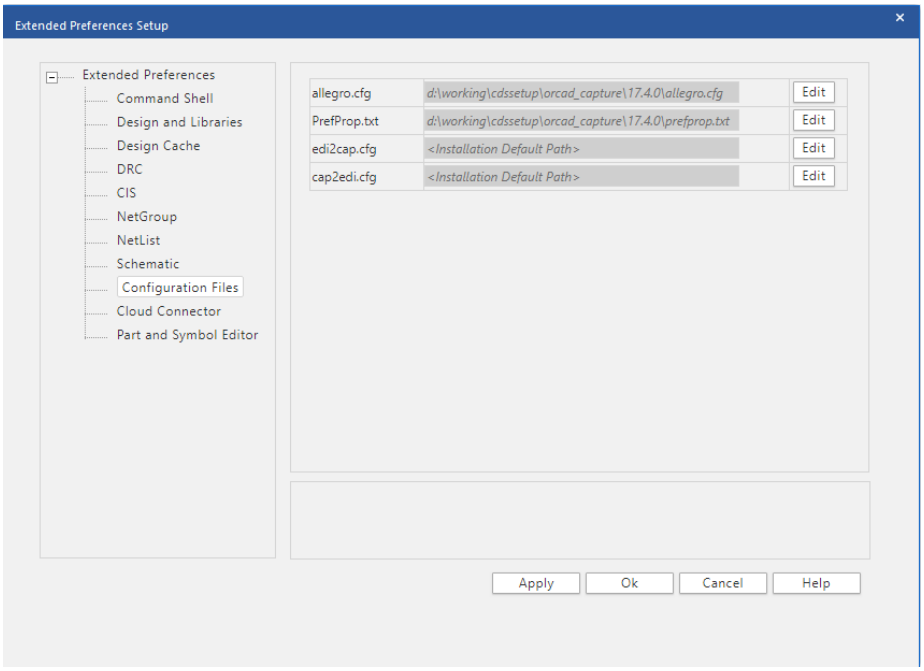


Add the following entry to the [pinprops] section. NET_SHORT=YES (if required).

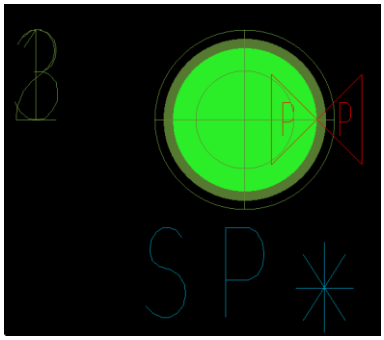


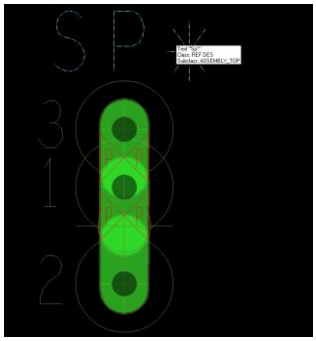
Save and close the allegro.cfg file and run Design Sync as you would normally.

There is an option in OrCAD Capture that will allow you to store the allegro.cfg file in a user defined location. Use Options > Extended Preferences > Configuration Files then, Edit the location for the allegro.cfg file. This is stored as part of the capture.ini file and will be set for future use.

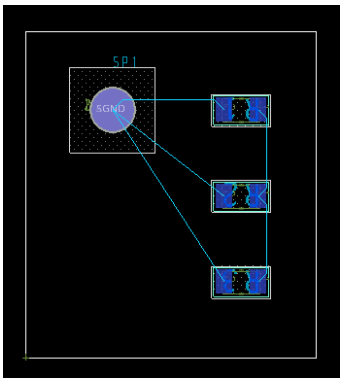


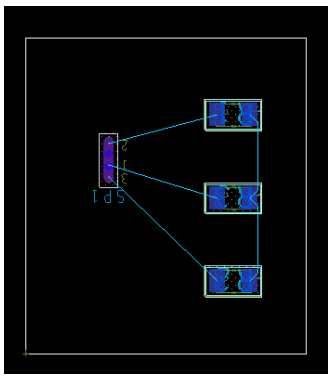
We can now create a net short footprint part for this schematic symbol. Open PCB Editor and create a new package symbol. For the footprint you have several options. You can either add three pins that use an oblong shaped pad which creates the short or just add three pads on top of each other. Both options are shown below as examples. You will get DRC's in the symbol mode, these will be corrected once the netlist is imported into the PCB.





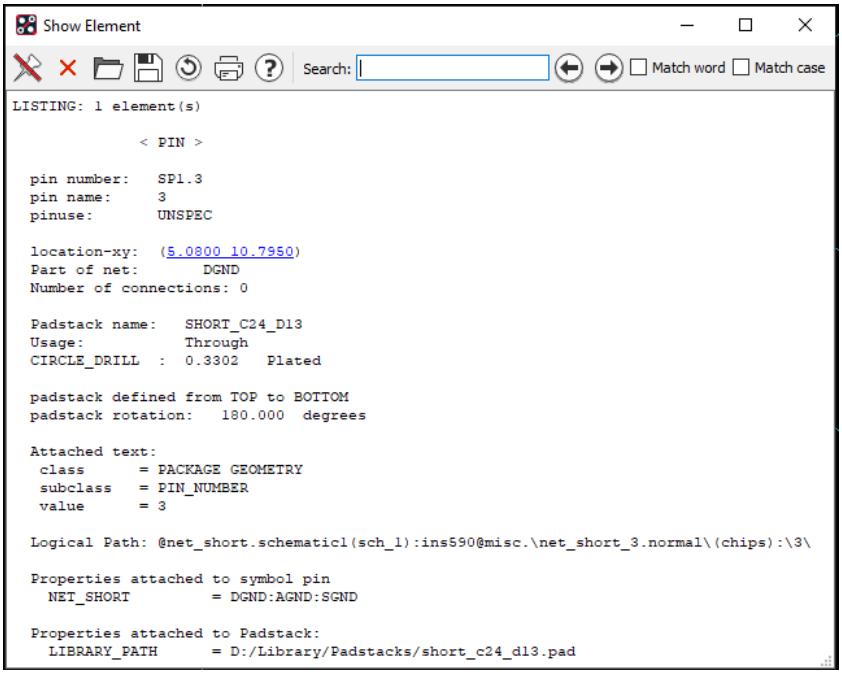
Open the board file and import the netlist from Capture. Place your components. You will notice in the next screenshot that the net short SP1 is placed and there are no DRC errors.



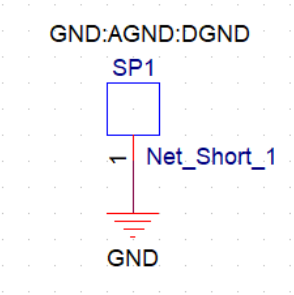


There are advantages and disadvantages to either footprint, the first uses less real estate but you will still get some DRC's if the three connections are routed on the same layer (ideal for multi-layer boards). You will not get these DRC's if you use the second option, but it does take up more real estate.

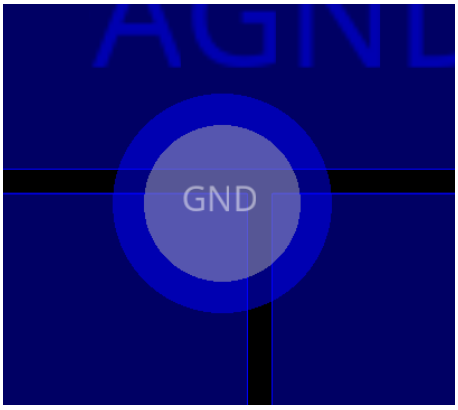
The final view below shows a show element view of one of the net short pins. You can see the NET_SHORT property applied to the pin.



The second option for creating a netshort that only uses a single pin in the schematic and one Pad in the PCB. The biggest advantage of this solution is that the real estate used on the board is much smaller and on many modern designs having a single point solution can give better results for the PCB. The picture below shows the schematic symbol which is a single pin connected to one of the required connections (The example below uses GND as the main connection). The disadvantage of this schematic view is that you do not graphically see the netshort physically connected to the different nets as you do in the other two examples above, you are relying on the NET_SHORT property display for the shorting information.

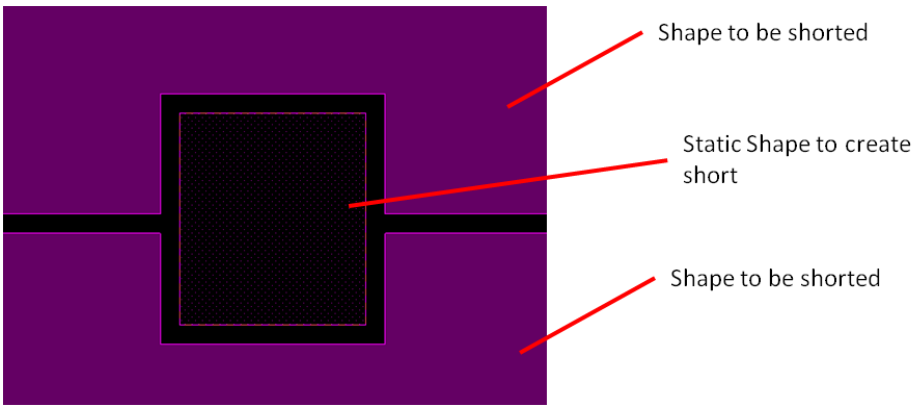


For the PCB only a single PAD is used and in the picture below shows the pad crossing the boundary of the three nets GND, GND_EARTH and AGND. This example also means that there are no extra DRC's that need to be waived or extra properties required but the main disadvantage of this is that there is only one connection for this pin (GND). This means that you will have no feedback whether you make the short to AGND and GND_EARTH.

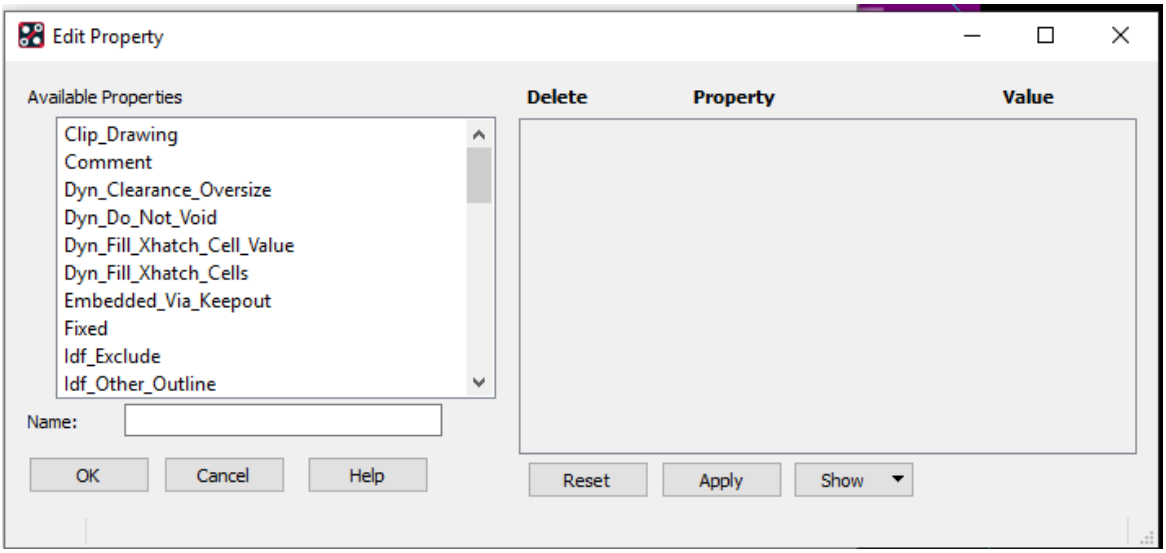


The final option does not use a pin or pins to create the net short but simply a small area of copper. You can add a static shape copper area to create the short between two other shapes on a specific layer of the PCB. The steps are described below.

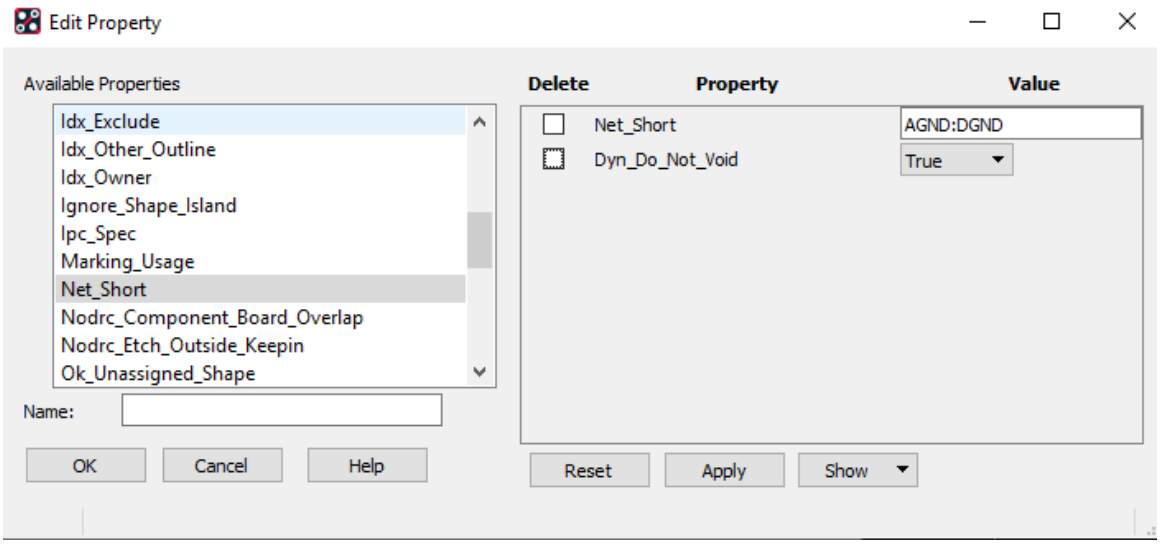
Draw a static shape on the layer and area required, naturally the shape is automatically voided from any dynamic shapes based on the dynamic copper clearances. You will see something similar to the following:-



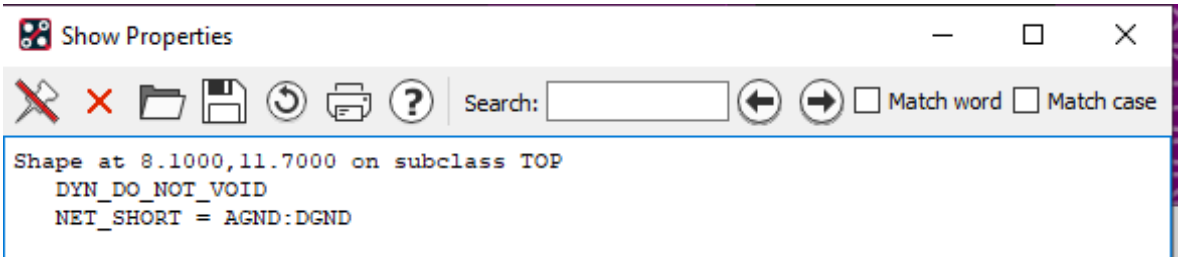
You now need to add properties to the static shape to create the required effect. To do this use Edit > Properties (Allegro) or Edit > Object Properties (OrCAD) then making sure you have Shapes selected in the Find Filter, select the static shape with a left click, you will see the following property edit window:-



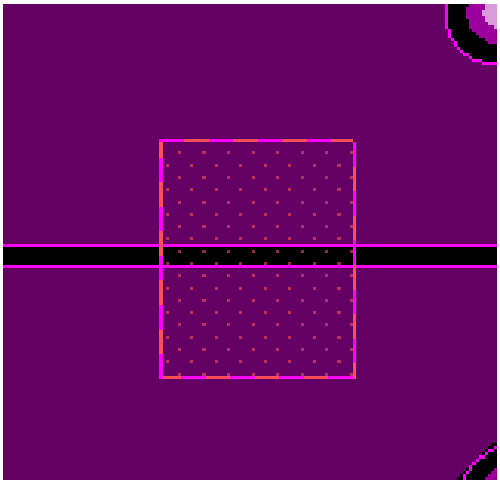
Locate the property name Dyn_Do_Not_Void and click on Apply. This property is added to stop the dynamic shapes from voiding the static one. Locate the property Net_Short and left click to select the property, you now need to add the two net names you wish to short together in the format netname1:netname2, for this example it's AGND:DGND.



Click on Apply and the Show Properties window will now show the properties applied to the shape.



Close both the Property Editor and Show Properties window. The resulting shape will look like the following:-



If the shapes do not update dynamically you may need to update the shapes to refresh the display. Use Shape > Global Dynamic Params > Shape Fill tab and click on Force Update or use Display > Status (Allegro) or Check > Design Status (OrCAD) and click on Update Shapes.