Introduction

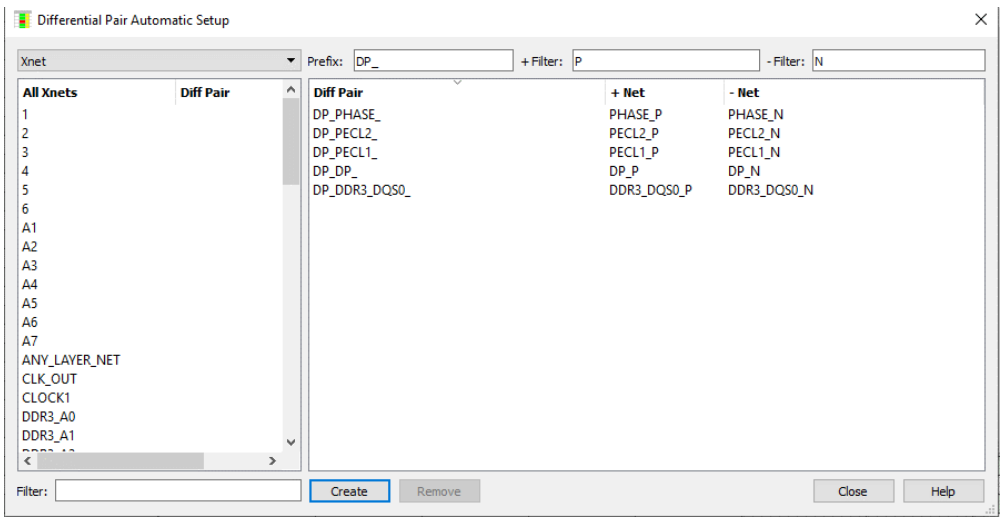
A differential pair is a pair of conductors used for differential signalling. Differential pairs are usually found on a printed circuit board, in cables (twisted-pair cables, ribbon cables), and in connectors. The term can also refer to a pair of transistors used as the input stage of a differential amplifier. By using this technique minimises crosstalk and electromagnetic interference, both noise emission and noise acceptance, and can achieve a constant and/or known characteristic impedance, allowing impedance matching techniques is important in a high-speed signal transmission line or high quality balanced line and balanced circuit audio signal path. This technical note covers: -

- Auto Generation of Diff Pair Objects
- Grouping Diff Pairs with Net Classes
- Driving rules with the Physical CSET including Min Line Space and Tolerance
- Region support for Diff Pair Line Width and Gap
- Setting up Electrical Rules (Uncoupling, Phase, Relative Delay)

How to Define Differential Pairs.

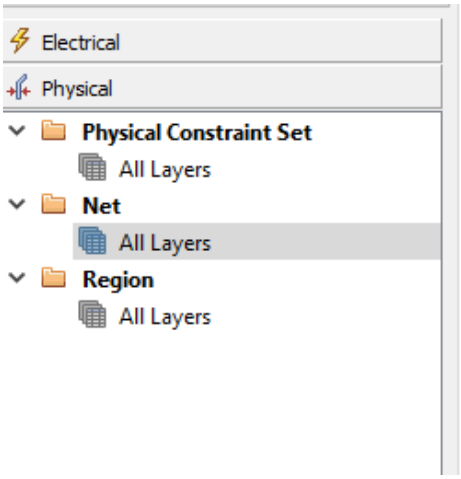
It should be noted that any level of the Cadence PCB Tools can generate differential pairs but for certain rules you may need to use a different license (Dynamic Phase for example).

We start by defining the differential pairs in the design. Just to note differential pairs can be setup in the schematic (Tools > Create > Differential Pair or via Constraint Manager in OrCAD Capture) and are defined in Constraint Manager when imported via design sync, or they can be setup manually using Setup>Constraints>Constraint Manager (Allegro) or Setup>Constraints (OrCAD) which launches Constraint Manager. Select the Electrical>Net>Routing>Differential Pair folder then use Objects>Create>Differential Pair. Select Auto Setup. The following GUI will appear: -



For this example, I have used Prefix = DP_; + filter = P; - filter = N. Nets with a common root name with suffixes P and N will be listed. Select Create then Close the remaining forms. This is used to sort through the net names and locate your differential pairs. Use suitable prefixes and filters for your design.

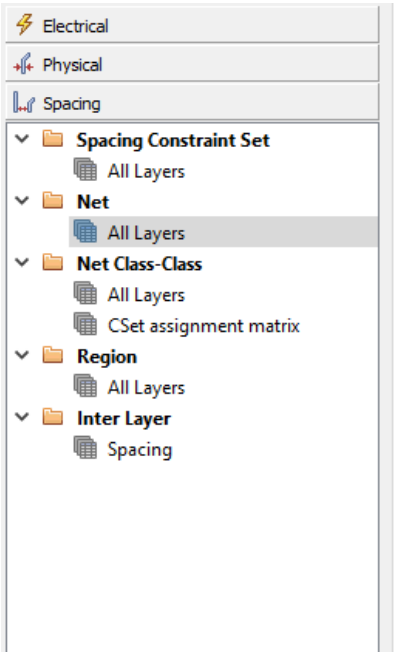
Click on the Physical domain>Net>All Layers Workbook noting the newly created Diff Pair (DPr) Objects.



diffpairs

Objects			Referenced Physical CSet
Type	S	Name	
*	*	*	*
Dsn		diffpairs	DEFAULT
NCls		DP_CLASS(5)	DEFAULT
DPr		DP_DDR3_DQS0_	DEFAULT
DPr		DP_DP_	DEFAULT
DPr		DP_PECL1_	DEFAULT
DPr		DP_PECL2_	DEFAULT
DPr		DP_PHASE_	DEFAULT

Now Create a Net Class for the Diff Pairs. With the left click select/drag the 3 Diff Pair Objects then right click > Create > Class. For this example, the name of DP_CLASS is used. This step can also take place in the Spacing Domain. Net Classes allow us to apply constraints at the top of the hierarchy. Net Classes will be used to create spacing rules between the DP_CLASS and will also be used in a Region application later in this note.



Objects			Referenced Spacing CSet	Line To	Thru Pin To
Type	S	Name		All	All
				mm	mm
*	*	*	*	*	*
Dsn		diffpairs	DEFAULT	0.1016	***
NCls		DP_CLASS(5)	DEFAULT	0.1016	***
DPr		DP_PHASE_	DEFAULT	0.1016	***
Net		PHASE_P	DEFAULT	0.1016	***
Net		PHASE_N	DEFAULT	0.1016	***
DPr		DP_PECL2_	DEFAULT	0.1016	***
Net		PECL2_P	DEFAULT	0.1016	***
Net		PECL2_N	DEFAULT	0.1016	***
DPr		DP_PECL1_	DEFAULT	0.1016	***
Net		PECL1_P	DEFAULT	0.1016	***
Net		PECL1_N	DEFAULT	0.1016	***
DPr		DP_DP_	DEFAULT	0.1016	***
Net		DP_P	DEFAULT	0.1016	***
Net		DP_N	DEFAULT	0.1016	***
DPr		DP_DDR3_DQS0_	DEFAULT	0.1016	***
Net		DDR3_DQS0...	DEFAULT	0.1016	***
Net		DDR3_DQS0...	DEFAULT	0.1016	***

Next, we define the Diff Pair Physical Rules. Under Physical domain>Physical Constraint Set > All Layers create a new Physical CSet called DP100. To do this Click on the Default CSet then right click > Create > Physical CSet. Enter the name DP100 then add the following values for the DP100 rule. You will need to expand the + next the DP100 name to enter the alternate layer rules.

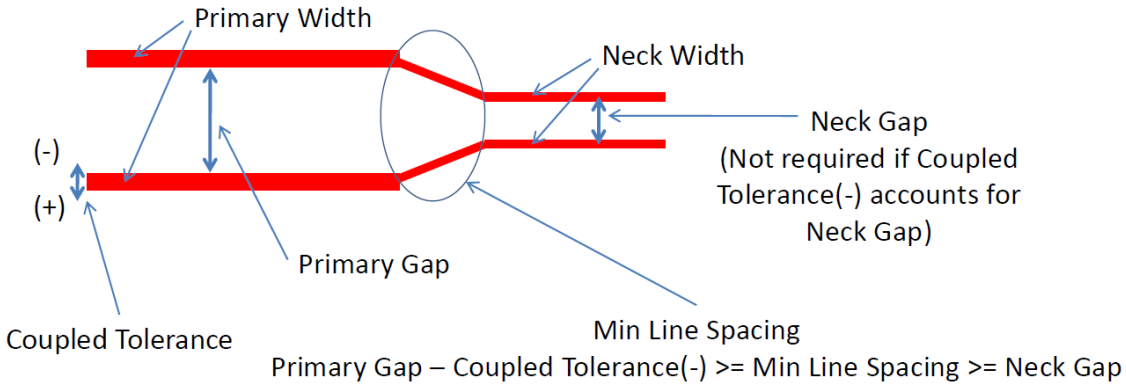
a. Min Line Width 0.2mm for outer layers, 0.15mm for inner layers.
b. Primary Gap 0.2mm for outer layers, 0.15mm for inner layers.
c. +/- Tolerance 0.05mm for all layers.
d. Min Line Space 0.15mm for outer layers, 0.1mm for inner layers.

Objects			Referenced Physical CSet	Line Width		Neck		Differential Pair				
Type	S	Name		Min	Max	Min Width	Max Length	Min Line Spacing	Primary Gap	Neck Gap	(+)Tolerance	(-)Tolerance
				mm	mm	mm	mm	mm	mm	mm	mm	mm
*	*	*	*	*	*	*	*	*	*	*	*	*
Dsn		diffpairs	DEFAULT	0.1270	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000
PCS		DEFAULT		0.1270	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000
PCS		DP100		0.2000:0.1500:...	0.0000	0.0000	0.0000	0.1500:0.1000:...	0.2000:0.1500:...	0.0000	0.0500	0.0500
LTyp		Conductor		0.1500	0.0000	0.0000	0.0000	0.1000	0.1500	0.0000	0.0500	0.0500
Lyr	1	TOP		0.2000	0.0000	0.0000	0.0000	0.1500	0.2000	0.0000	0.0500	0.0500
Lyr	2	SIGNAL_2		0.1500	0.0000	0.0000	0.0000	0.1000	0.1500	0.0000	0.0500	0.0500
Lyr	3	SIGNAL_3		0.1500	0.0000	0.0000	0.0000	0.1000	0.1500	0.0000	0.0500	0.0500
Lyr	4	SIGNAL_4		0.1500	0.0000	0.0000	0.0000	0.1000	0.1500	0.0000	0.0500	0.0500
Lyr	5	SIGNAL_5		0.1500	0.0000	0.0000	0.0000	0.1000	0.1500	0.0000	0.0500	0.0500
Lyr	6	SIGNAL_6		0.1500	0.0000	0.0000	0.0000	0.1000	0.1500	0.0000	0.0500	0.0500
Lyr	7	SIGNAL_7		0.1500	0.0000	0.0000	0.0000	0.1000	0.1500	0.0000	0.0500	0.0500
Lyr	8	BOTTOM		0.2000	0.0000	0.0000	0.0000	0.1500	0.2000	0.0000	0.0500	0.0500
LTyp		Plane		0.1500	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000

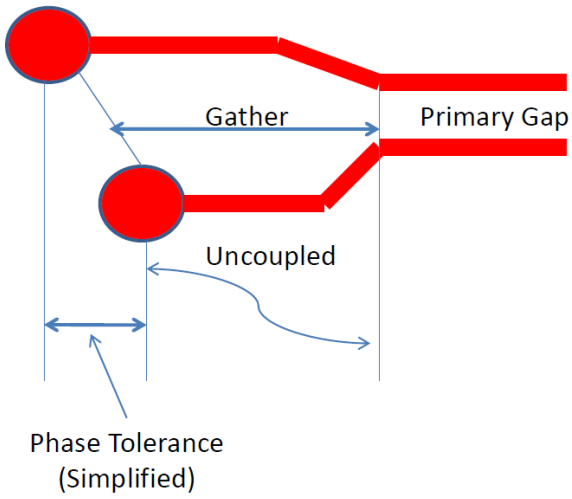
Note on Min Line Space and Tolerance - Use primary or neck gap, whatever is lower minus the negative tolerance value. In the above example: -

Min line space (outers) = 0.2 – 0.05 = 0.15mm
Min line space (inners) = 0.15 – 0.05 = 0.1mm

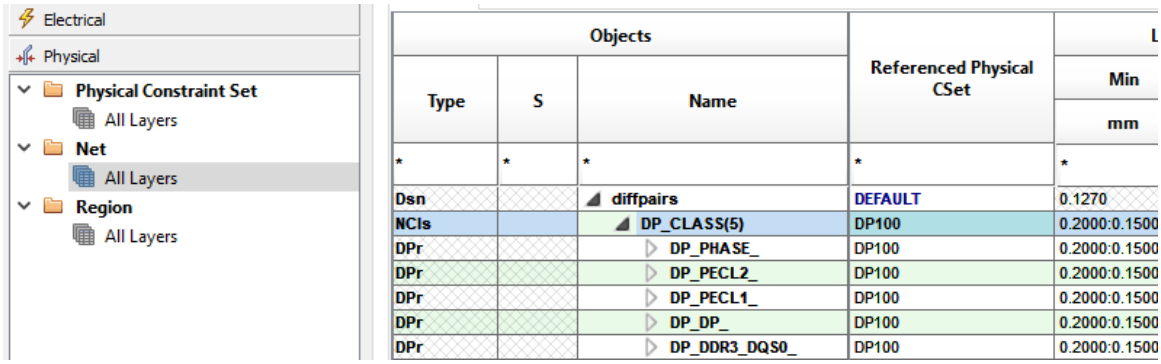
A Min Line Space DRC is reported if the Diff Pair Gap is below 0.15mm outers and 0.1mm inners. If the Min Line Space is left blank, the Diff Pair Gap will be derived from the line to line spacing rule used in the Spacing domain. The following two figures show a graphical representation of the basic settings for a differential pair.



Pair is Uncoupled
IF (Gap < Primary Gap – Coupled Tolerance(-))
OR (Gap > Primary Gap + Coupled Tolerance(+))
OR (Gap < Neck Gap)

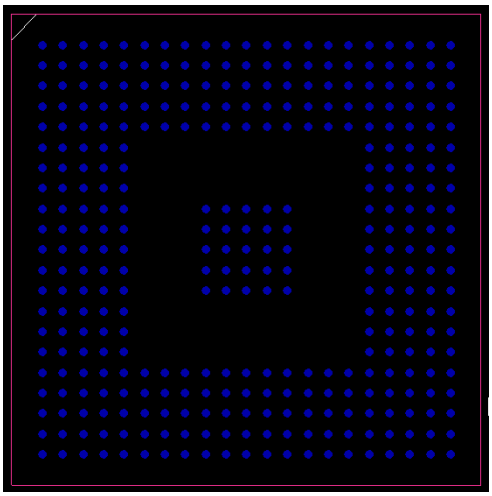


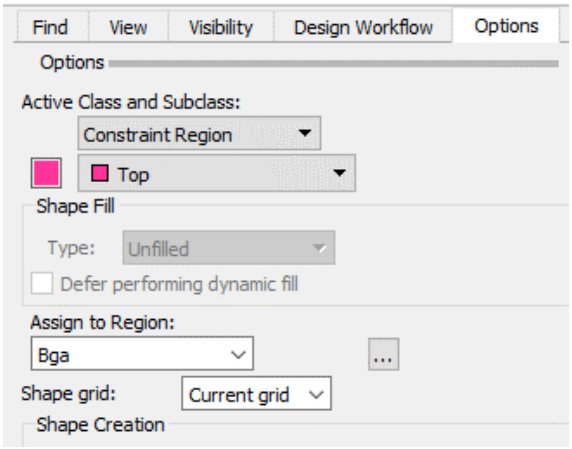
Now apply the new Physical CSet to the Net Class DP_CLASS. Click on Net > All Layers workbook in the Physical Domain and Click on the Referenced Physical CSet cell adjacent to the DP_CLASS and select DP100 from the drop-down list.



Differential Pairs can be defined as an Electrical CSet or a Physical CSet. You can define Min Line Spacing, Primary Gap, Primary Width, Neck Gap, Neck Width, + and – Tolerance as either a Physical or Electrical CSet. The differences being that if you wish to change the track thickness and spacing as the differential pair changes layers in the PCB to control impedance then they should be defined as a Physical CSet. If the track thickness and gap remain the same throughout the cross section of the PCB then it is recommended that the differential pair be defined as an Electrical CSet. This is also true if you wish to use Constraint Regions to control a different set of design rules by area e.g. smaller track and gap widths. For Constraint Regions the differential pairs MUST be defined as a Physical CSet. Uncoupled length and phase (static and dynamic) must be defined as an Electrical CSet so you may find you have both an Electrical CSet and a Physical CSet to control the differential pairs. You will see the values for Min Line Spacing, Primary Gap, Primary Width, Neck Gap, Neck Width, + and – Tolerance will be inherited from the Physical / Electrical domains depending on how they are defined.

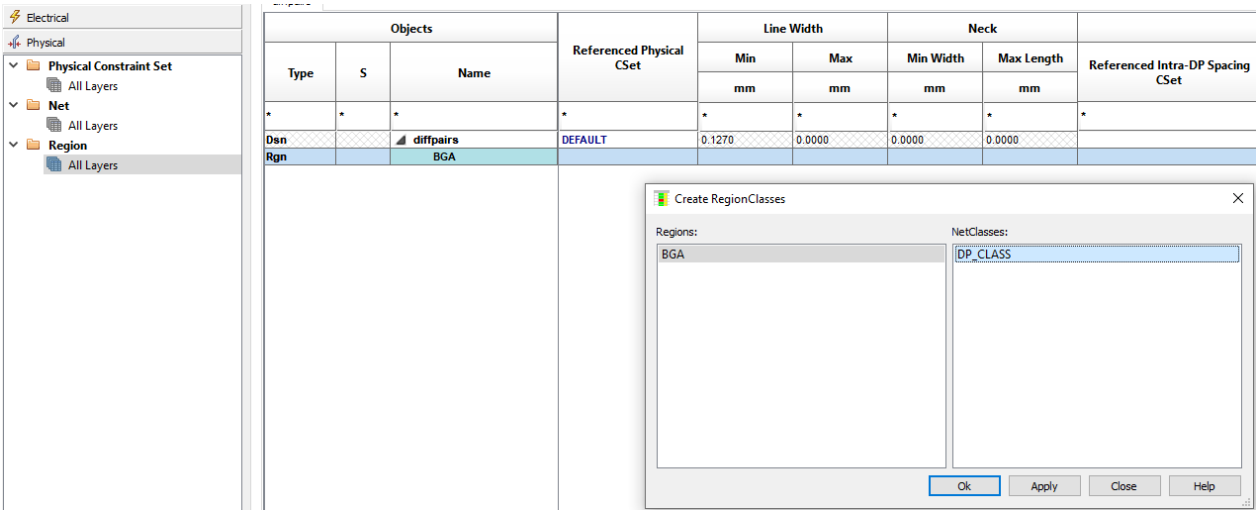
As part of designs that use BGA's PCB Editor (Allegro or OrCAD Professional) gives users the option to define a Constraint Region around the BGA then have a different set of design rules that control that area e.g. smaller track and gap widths. To do this in the PCB Editor main window (you can leave the Constraint Manager window open). Zoom into the area where the BGA's are located, for this example we are going to add a Constraint Region Shape to the top side of the board. Use Shape>Rectangular, from the Options menu set the class / subclass to Constraint Region / Top. Enter a Region name of BGA in the Assign to Region field, then draw a rectangle around the BGA using either the left click or the right click>Snap Pick to function.



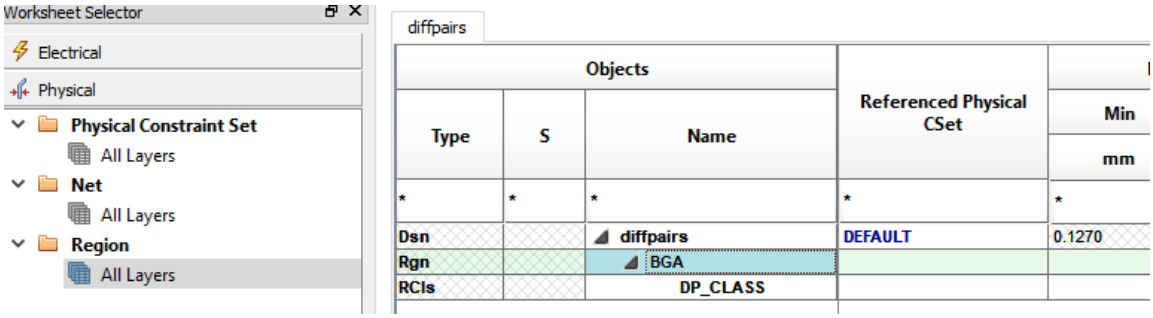


Once the Region has been defined, open Constraint Manager and Click on the Region>All Layers Workbook in the Physical Domain. We wish to use the Region to control just the differential pair line width and gap, not all signals

that cut across it. This is best solved by the use of a “Region Class” Constraint object. Select the BGA Region then use right click>Create>Region-Class.



From the popup GUI, select the Net Class DP_Class then click OK.



The “Region-Class” (RCls) is slightly indented from the “Region” object BGA. The constraints assigned to the “Region-Class” take precedence over constraints assigned to the “Region” object (BGA).

There are now two options to consider:

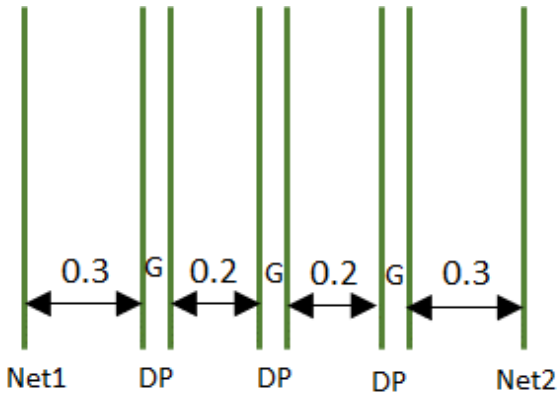
i. Create and assign a Physical CSet to the “Region-Class”

ii. Directly set values (also called an override)

We will directly set the values on the basis of there are only 3 constraints involved and no variance is required across layers. Enter 0.1mm for Min Line Width, 0.1mm for Primary Gap and 0.05mm for Min Line Spacing (0.1 Region Gap - 0.05 Tolerance). Click NO to any assertion message that may appear when entering in values for gap and min line space.

Objects			Referenced Physical CSet	Line Width		Neck		Differential Pai		
Type	S	Name		Min	Max	Min Width	Max Length	Referenced Intra-DP Spacing CSet	Min Line Spacing	Primary Gap
				mm	mm	mm	mm		mm	mm
*	*	*	*	*	*	*	*	*	*	*
Dsn		diffpairs	DEFAULT	0.1270	0.0000	0.0000	0.0000		0.0000	0.0000
Rgn		BGA								
RCls		DP_CLASS		0.1000					0.0500	0.1000

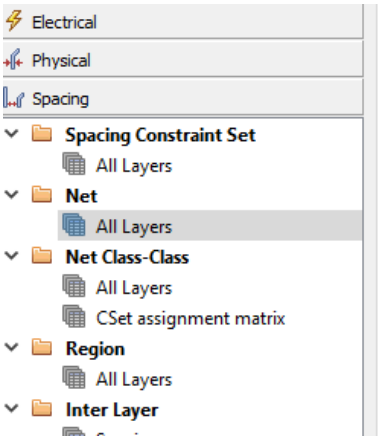
Next we are going to define the Diff Pair general Spacing Rules. The following figure represents the spacing rules required for this example between Diff Pairs and other nets. Diff Pairs are required to be spaced at 0.2mm to each other and 0.3mm to other nets. The Primary Gap was set in the previous steps. See the Physical Constraint setup above.



We start by creating a new Spacing CSet called DP100_0.2 Click on the Default CSet then right click > Create > Spacing CSet. Enter name DP100_0.2. Change the Line to Line space to 0.2mm. Now create another Spacing CSet called DP100_0.3. Change Line to Line space to 0.3mm. The figure below shows the Spacing CSets defined.

Objects			Referenced Spacing CSet	Line To					
Type	S	Name		All	Line	Thru Pin	SMD Pin	Test Pin	Th
				mm	mm	mm	mm	mm	
*	*	*	*	*	*	*	*	*	*
Dsn		diffpairs	DEFAULT	0.1016	0.1016	0.1016	0.1016	0.1016	0.1016
SCS		DEFAULT		0.1016	0.1016	0.1016	0.1016	0.1016	0.1016
SCS		DP100_0.2		***	0.2000	0.1016	0.1016	0.1016	0.1016
SCS		DP100_0.3		***	0.3000	0.1016	0.1016	0.1016	0.1016

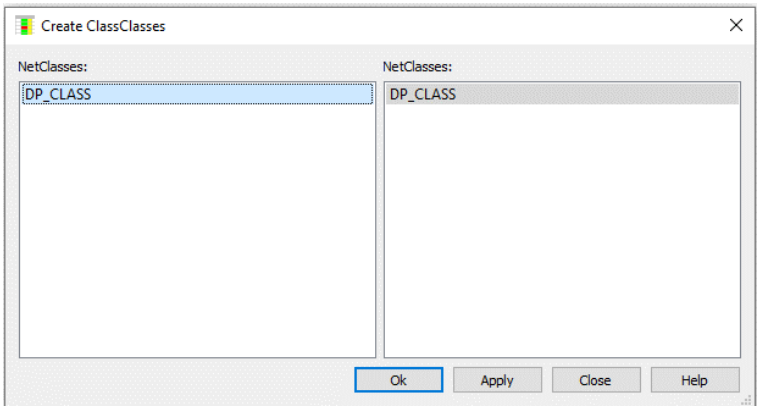
Assign the Spacing CSet DP100_0.3 to the Net Class DP_CLASS. This rule sets a 0.3mm line to line space from the Diff Pair objects to all other nets.



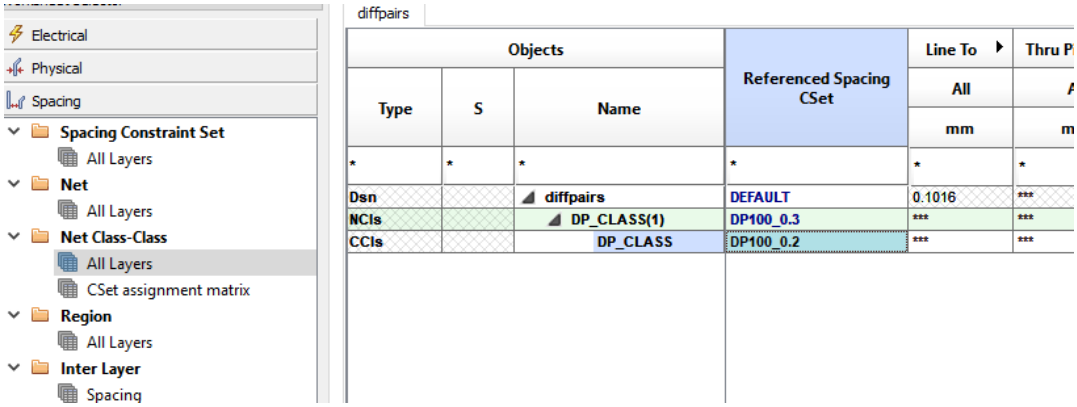
Objects			Referenced Spacing CSet	Line To	Thr
Type	S	Name		All	
				mm	
*	*	*	*	*	*
Dsn		diffpairs	DEFAULT	0.1016	***
NCls		DP_CLASS(5)	DP100_0.3	***	***
DPr		DP_DDR3_DQS0_	DP100_0.3	***	***
DPr		DP_DP_	DP100_0.3	***	***
DPr		DP_PECL1_	DP100_0.3	***	***
DPr		DP_PECL2_	DP100_0.3	***	***
DPr		DP_PHASE_	DP100_0.3	***	***
Net		ANY_LAYER_NET	DEFAULT	0.1016	***
Net		A1	DEFAULT	0.1016	***

Now create a Net Class-Class object. A “Net Class-Class” object (NCC) is used to control line spacing between Net Classes; both inter and intra relationships. Click on the Net Class-Class > All layers workbook. Click on the Net

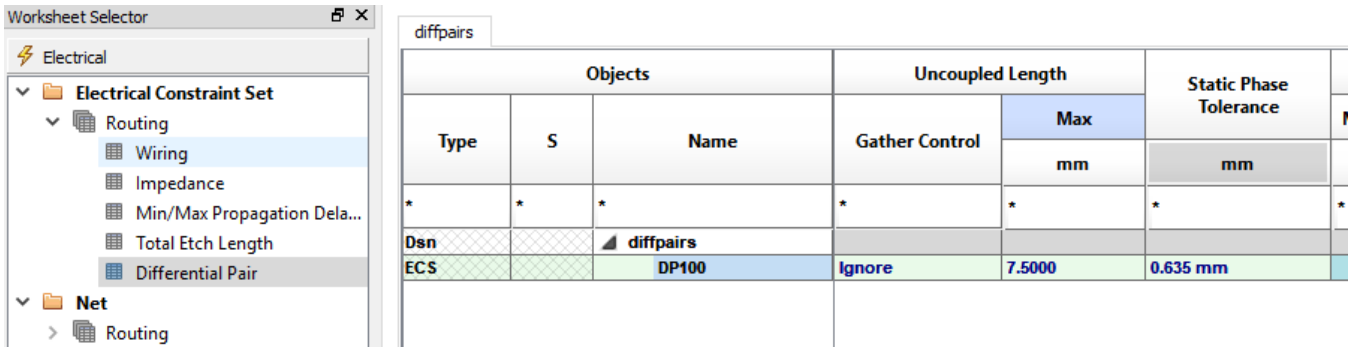
Class DP_CLASS then RMB>Create>Class-Class. Click Apply or OK to create the relationship that is presented in the GUI shown below.



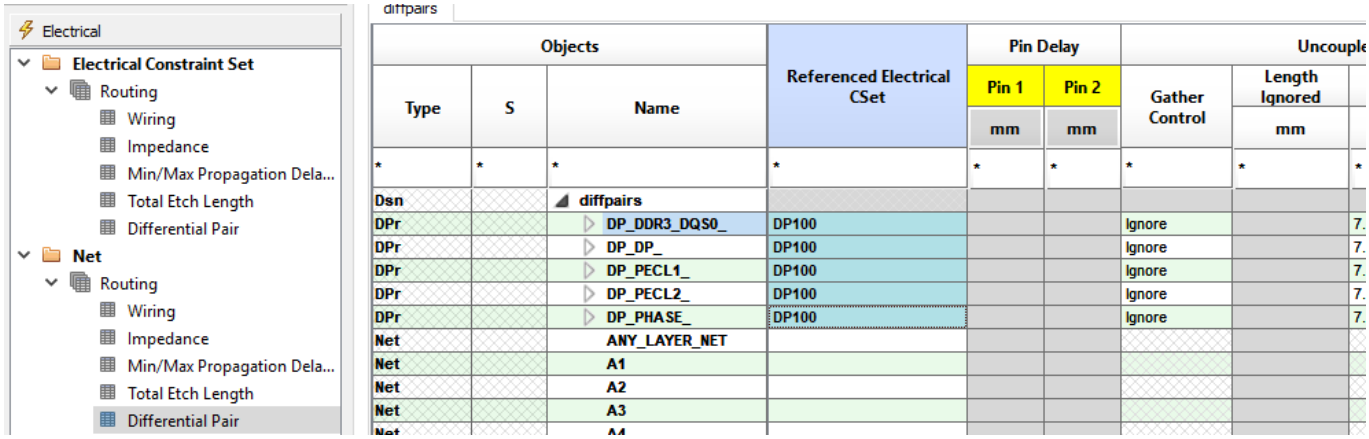
Assign the CSET DP100_0.2 to the NCC object as shown below.



Now we need to define the Electrical Rule Setup (Uncoupling and Phase Control). Click on the Electrical Domain > Electrical Constraint Set > Diff Pair Worksheet. Create an Electrical CSet called DP100. Enter Gather Control = Ignore; Uncoupled Max Length = 7.5mm and Static Phase Tolerance = 0.635mm. Leave all other cells blank as we are using the Physical CSET to drive these rules and dynamic phase will be discussed later. If values are entered in the Electrical CSet, they will take precedence over rules set from a Physical CSet.



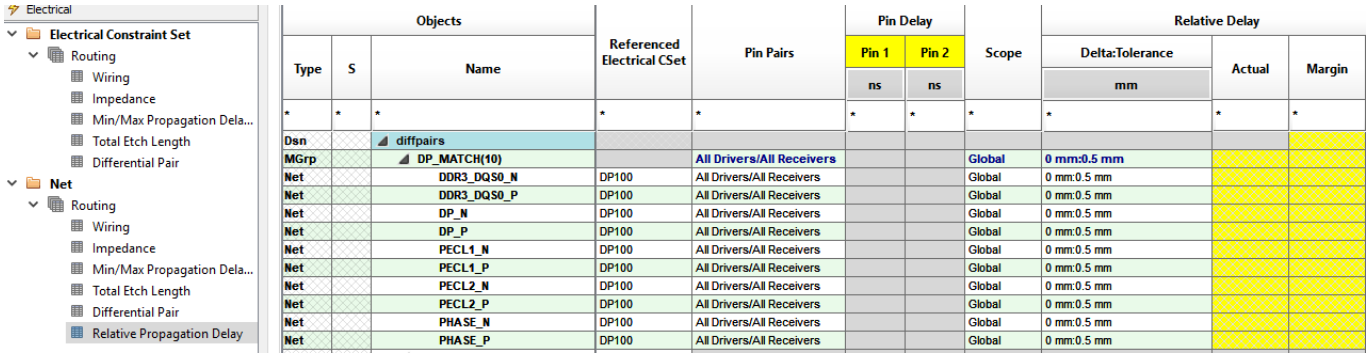
Apply the ECSet DP100 to the Diff Pairs. Click on the Net > Diff Pair Worksheet and Apply the ECSet DP100 to the 5 Diff Pairs.



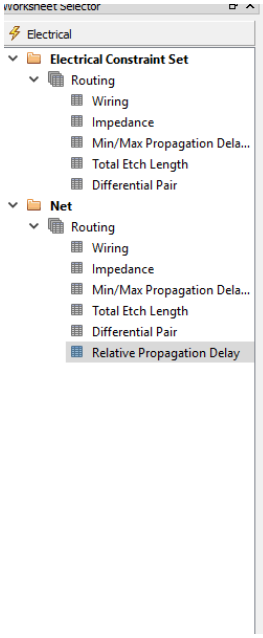
Electrical Rule Setup

Cadence OrCAD PCB Designer Professional and Allegro PCB Designer

Using an Electrical Rule Setup (Matched Group). Click on the Net > Relative Propagation Delay Worksheet. Expand each of the 4 Diff Pairs to see their net members then select each net with the left click. Use the Control key to extend the selection. Once the 10 nets are selected, use the right click>Create>Matched Group command then for this example enter a name of DP_MATCH. Working on the Matched Group row, enter Pin Pairs = All Drivers/All Receivers, Scope = Global and Delta:Tolerance = 0:0.5mm.



Since the Diff Pairs are not routed, the Actual and Margin cells appear in Yellow. DRC results based on actual unrouted lengths can be produced by setting the Unrouted Relative Delay DRC followed by an update of the DRC system. To enable the DRC from Constraint Manager, go to Analyze>Analysis Modes>Electrical, then enable the "Relative propagation delay in the DRC unrouted section. Constraint Manager will now show the match group updated with green and red bars. A Target is automatically assigned to the member of the group with the longest Manhattan length. The setup is now complete. You can route the differential pairs, get real time feedback whilst routing to meet the constraints defined.

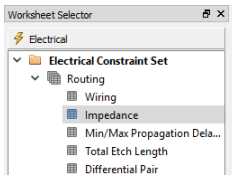


diffpairs

Objects			Referenced Electrical CSet	Pin Pairs	Pin Delay		Scope	Relative Delay			
Type	S	Name			Pin 1	Pin 2		Delta:Tolerance	Actual	Margin	+/-
					ns	ns		mm			
*	*	*	*	*	*	*	*	*	*	*	*
Dsn		diffpairs								75.3142 mm	
MGrp		DP_MATCH(10)		All Drivers/All Receivers			Global	0 mm:0.5 mm		75.3142 mm	
Net		DDR3_DQS0_N	DP100	All Drivers/All Receivers			Global	0 mm:0.5 mm		75.0642 mm	
RePP		U10.B1:U5.G17					Global	0 mm:0.5 mm	75.5642 mm	75.0642 mm	-
Net		DDR3_DQS0_P	DP100	All Drivers/All Receivers			Global	0 mm:0.5 mm		75.3142 mm	
RePP		U5.G18:U10.B2					Global	0 mm:0.5 mm	75.8142 mm	75.3142 mm	-
Net		DP_N	DP100	All Drivers/All Receivers			Global	0 mm:0.5 mm		69.0173 mm	
RePP		U18.19:U5.D15					Global	0 mm:0.5 mm	69.5173 mm	69.0173 mm	-
Net		DP_P	DP100	All Drivers/All Receivers			Global	0 mm:0.5 mm		69.2174 mm	
RePP		U18.20:U5.D16					Global	0 mm:0.5 mm	69.7174 mm	69.2174 mm	-
Net		PECL1_N	DP100	All Drivers/All Receivers			Global	0 mm:0.5 mm		70.4633 mm	
RePP		U17.3:U3.11					Global	0 mm:0.5 mm	70.9633 mm	70.4633 mm	-
RePP		U17.3:U11.10					Global	0 mm:0.5 mm	22.0561 mm	21.5561 mm	-
Net		PECL1_P	DP100	All Drivers/All Receivers			Global	0 mm:0.5 mm		23.486 mm	
RePP		U1.12:U11.9					Global	0 mm:0.5 mm	TARGET		
RePP		U3.10:U11.9					Global	0 mm:0.5 mm	12.6284 mm	12.1284 mm	-
RePP		U17.26:U11.9					Global	0 mm:0.5 mm	23.986 mm	23.486 mm	-
Net		PECL2_N	DP100	All Drivers/All Receivers			Global	0 mm:0.5 mm		37.8497 mm	
RePP		U17.17:U11.13					Global	0 mm:0.5 mm	38.3497 mm	37.8497 mm	-
Net		PECL2_P	DP100	All Drivers/All Receivers			Global	0 mm:0.5 mm		66.6213 mm	
RePP		U18.16:U11.12					Global	0 mm:0.5 mm	48.7637 mm	48.2637 mm	-
RePP		U20.15:U11.12					Global	0 mm:0.5 mm	27.6812 mm	27.1812 mm	-
RePP		U20.15:U18.16					Global	0 mm:0.5 mm	67.1213 mm	66.6213 mm	-
Net		PHASE_N	DP100	All Drivers/All Receivers			Global	0 mm:0.5 mm		56.0707 mm	
RePP		U5.D12:U12.3					Global	0 mm:0.5 mm	56.5707 mm	56.0707 mm	-
Net		PHASE_P	DP100	All Drivers/All Receivers			Global	0 mm:0.5 mm		54.4204 mm	
RePP		U12.2:U5.D11					Global	0 mm:0.5 mm	54.9204 mm	54.4204 mm	-

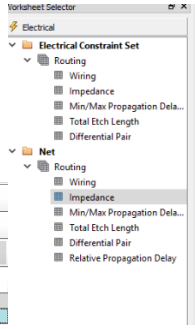
Adding Impedance Rules

Many differential pairs also require to be routed to a specific width to meet an impedance-based rule. OrCAD PCB Designer Professional and Allegro PCB Designer level licenses and above are able to do this. To add an impedance rule open Constraint Manager > Electrical > Electrical Constraint Set > Routing > Impedance and either create a new electrical CSet (ECS) or define the impedance and tolerance (either as a % or ohm) to an existing rule.



diffpairs

Objects			Single-line Impedance	
Type	S	Name	Target	Tolerance
			Ohm	Ohm
*	*	*	*	*
Dsn		diffpairs		
ECS		DP100	100	2 %

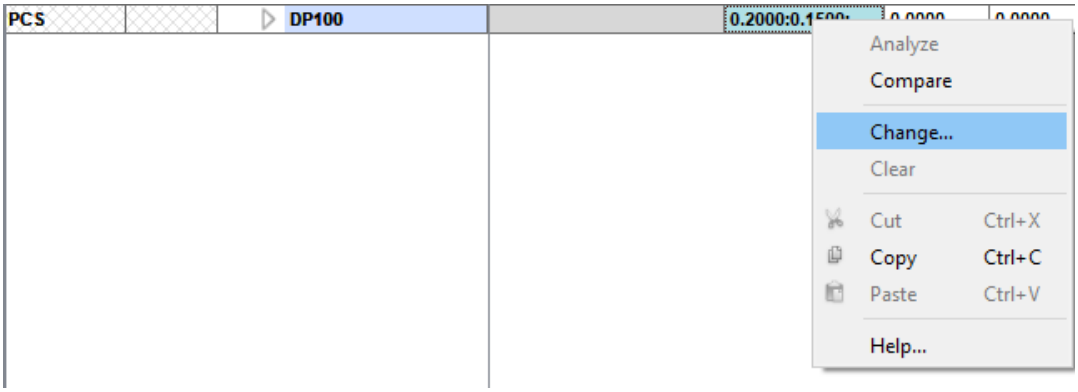


diffpairs

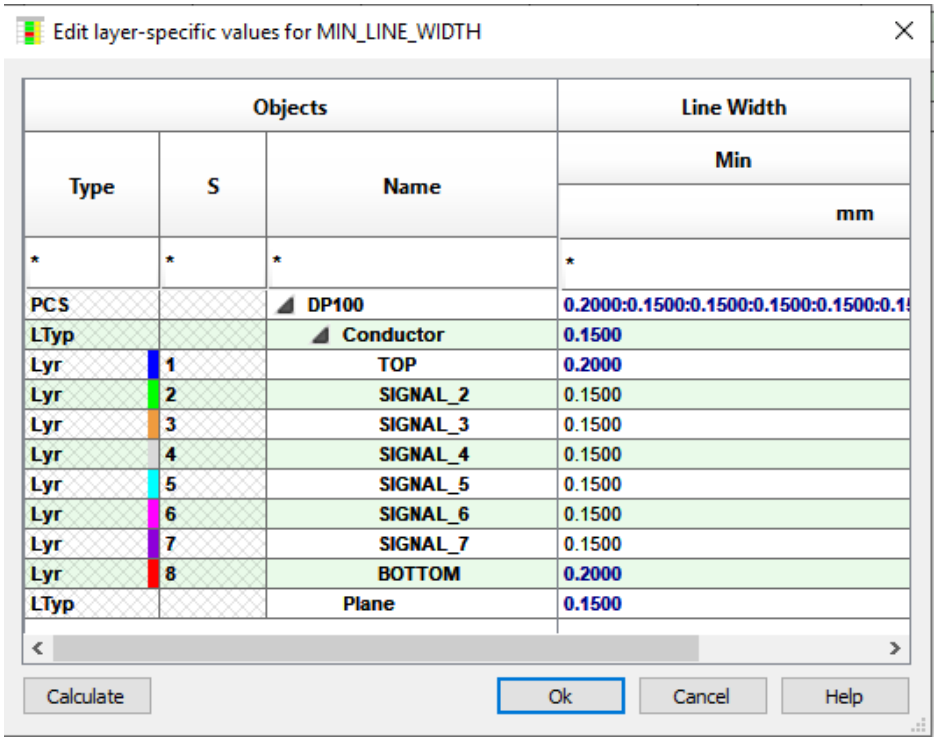
Objects			Referenced Electrical CSet	Single-line Impedance			
Type	S	Name		Target	Tolerance	Actual	Margin
				Ohm	Ohm	Ohm	Ohm
*	*	*	*	*	*	*	*
Dsn		diffpairs					
DPr		DP_DDR3_DQS0_	DP100	100	2 %		
Net		DDR3_DQS0_N	DP100	100	2 %		
Net		DDR3_DQS0_P	DP100	100	2 %		
DPr		DP_DP_	DP100	100	2 %		
Net		DP_N	DP100	100	2 %		
Net		DP_P	DP100	100	2 %		
DPr		DP_PECL1_	DP100	100	2 %		
Net		PECL1_N	DP100	100	2 %		
Net		PECL1_P	DP100	100	2 %		
DPr		DP_PECL2_	DP100	100	2 %		
Net		PECL2_N	DP100	100	2 %		
Net		PECL2_P	DP100	100	2 %		
DPr		DP_PHASE_	DP100	100	2 %		
Net		PHASE_N	DP100	100	2 %		
Net		PHASE_P	DP100	100	2 %		

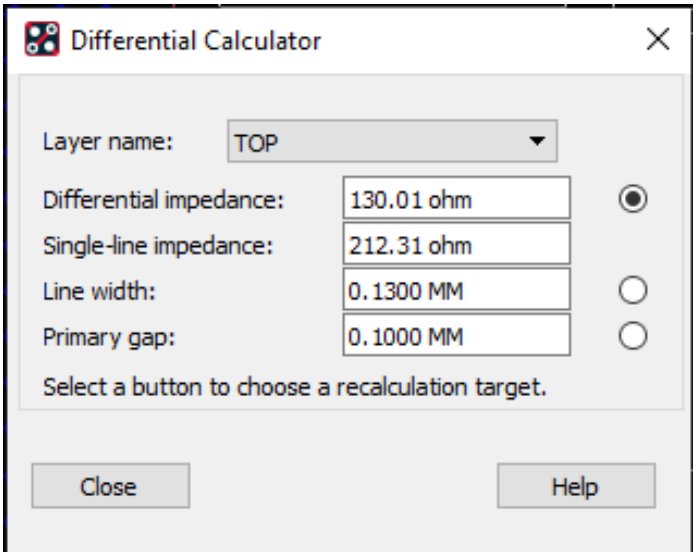
Once defined, the rules can be applied to the Nets > Impedance area of Constraint Manager as shown above right. You can now begin to route the differential pair. You will notice that because you have applied an impedance rule to the nets that the routing function behaves slightly differently because as you route PCB Editor invokes a 2D field solver to analyse the route thickness to ensure it meets the rules defined. Other points to note when using impedance based rules are that the Cross Section of the PCB **MUST** be defined accurately. The material, thickness, conductivity, dielectric constant and loss tangent can all affect the impedance rule. You **MUST** also define a suitable Shield layer. There are also options to setup Single and Differential Impedance, line thickness is calculated based on the values entered.

If you have access to an Allegro PCB Designer license you can use a Differential Impedance Calculator. To use this right click any field in the Physical domain (like Min Line Width) and choose Change.



The form that is shown is available in all license levels but the Calculator button is only available in Allegro.





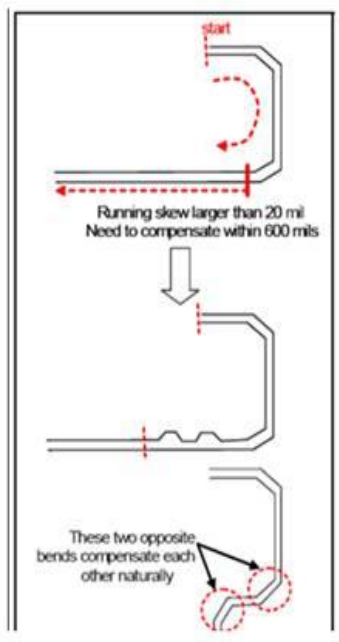
Note: - Many users of Impedance based traces often talk directly to the PCB Fabricator to confirm or indeed define the actual width of the trace that requires to be of a certain impedance. This is largely down to the fact

that PCB substrates often vary in performance and construction, pre-preg's used can also differ, all which have a huge effect on the actual impedance of a trace. Fabricators are responsible for manufacturing your finished PCB's so if they define the impedance trace width they often use tools based on their current stock material. If you prefer to use this flow, the MIN_LINE_WIDTH can be defined with this information meaning that you do not need to set up the impedance rules. Using a physical constraint rule will usually result in a much better routing performance since the 2D solver will not be running during the routing process.

Appendix

Note: - for Phase Tuning and Dynamic Phase you need either an Allegro PCB Designer or OrCAD Professional license (or higher).

Dynamic Phase Control for Differential Pairs



Differential Pair (Diff Pair) technology has evolved where more stringent checking is required in the area of phase control. This is evident on higher data rates associated with parallel buses such as QPI, SMI, PCI Gen 2, DDR, QDR and Infiniband. In the simplest of terms, Diff Pair technology is sending opposite and equal signals down a pair of traces. Keeping these opposite signals in phase is essential in assuring that they function as intended.

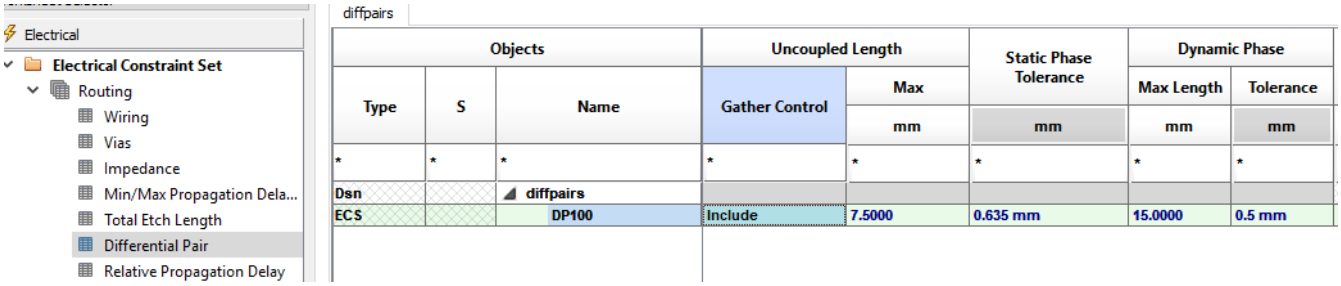
The Dynamic Phase check is designed to meet the guidelines that suggest that the path lengths of the true and complement signals within the differential pair must differ by no more than "x mils" along the entire path of the net. If at any point on the net, the skew between true and complement exceeds "x mils", this mismatch needs to be compensated within "y mils". Representative values for x and y might be x = 20 and y = 600.

The constraints associated with Differential Pairs support Static and Dynamic Phase. The margins of each constraint can be set independently using length or time. The Max Length (running skew) constraint for Dynamic Phase is limited to length only.

Static Phase Tolerance – a one-time check from Driver to Receiver comparing lengths or delay of each member. If a Driver cannot be determined, the check is performed across the longest path of the pair.

Dynamic Phase – Etch length of each member is compared at each bend point interval across the Driver-Receiver path of the Diff Pair. Etch length is always measured back to the Driver pins.

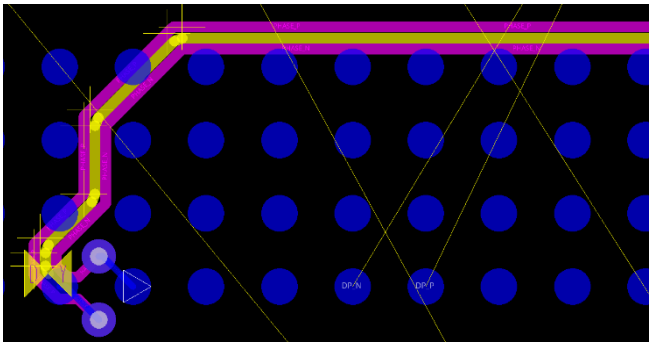
Dynamic Phase Max Length – When specified, the Diff Pair is permitted to exceed the phase tolerance constraint for a contiguous etch length of less than or equal to the value of Max Length specified. If no compensation is made within this specified distance, a DRC will be reported at the point where the Diff Pair first goes out of phase.



As an example, suppose your Dynamic Phase constraints are set as follows:

Static Phase Tolerance	Dynamic Phase	
	Max Length	Tolerance
mm	mm	mm
*	*	*
0.635 mm	7.5000	0.5 mm

When the DRC is updated, it shows the following:



The beginning of the yellow pseudo line (closest to driver) is where the Diff Pair initially goes out of Phase (beyond the 20 mil Static Phase tolerance). The DRC marker *D-Y* is placed at the initial 'out of phase spec' location as measured from the Driver Pins.

Notes:

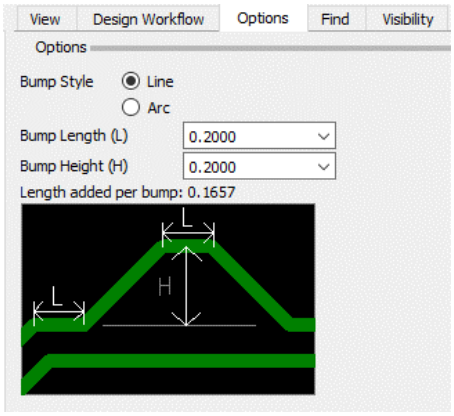
- There can only be 1 DRC marker on a pair, even though there may be multiple violation zones.
- It is assumed that the designer will correct the phase issues working from the Drivers to the Receivers.

Differential Phase Tuning

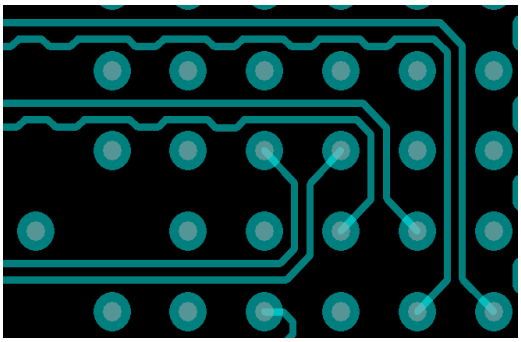
Phase Tuning is an alternative to using the mouse guided delay tune command and offers the precision of finite length adjustment to differential signals that are length/phase constrained. It is especially effective on static or dynamic phase-constrained Differential Pairs where iterative etch compensation may be required at various

points along the path of either member of the pair. Simply make a mouse click at any point on the cline path to add in a single-parameterized phase bump.

The command is located in the Route Menu of the PCB Editor. When invoked, parameters can be set in the Options panel. Select a style of Line or Arc then define its respective length/size parameters. The form will compute the added compensation for each bump before applying you it.



Phase Tune Options



Differential Phase Bumps