

Using Differential Pairs in Allegro PCB Editor

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Purpose

A differential pair represents a pair of Xnets or Nets routed differentially. The two members of a differential pair carry the opposite signals. This document covers various aspects of implementing differential pairs in Allegro PCB Editor.

Audience

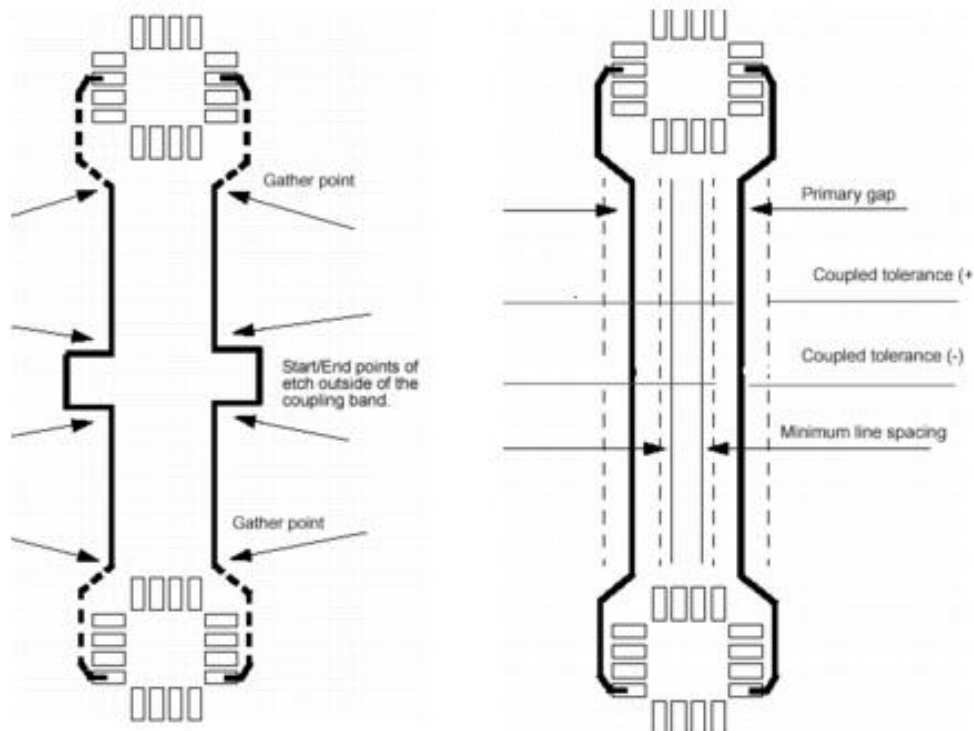
This document is intended for Allegro PCB Editor users who want to use differential pairs in Allegro PCB Editor.

Types of Differential Pairs

Model-defined differential pairs are ones in which the differential pair assignment is done in the IBIS model.

User-defined differential pairs can be defined in Allegro Design Entry HDL using the DIFFERENTIAL_PAIR property on nets, or can be created in Constraint Manager. For High Speed designs, it is recommended to use model-defined differential pairs.

Differential Pair Terminology



Primary Gap	Specifies the ideal edge-to-edge spacing between a pair of nets in the differential pair that should be maintained for the entire length of the pair.
Primary Width	Specifies the minimum width of each line of the differential pair.
Neck Gap	Specifies the edge-to-edge spacing between nets of a differential pair as it goes through tight areas.
Neck Width	Specifies the minimum allowable width for a line in a differential pair as it goes through tight areas.
Coupled Tolerance (+)	Specifies the allowable positive deviation from the Primary Gap for a differential pair to still be considered edge-coupled.
Coupled Tolerance (-)	Specifies the allowable negative deviation from the Primary Gap for a differential pair to still be considered edge-coupled.
Minimum Line Spacing	A line-to-line check to make sure that the other settings are not violated.

Creating a Differential Pair

This section covers the following two methods to create a differential pair.

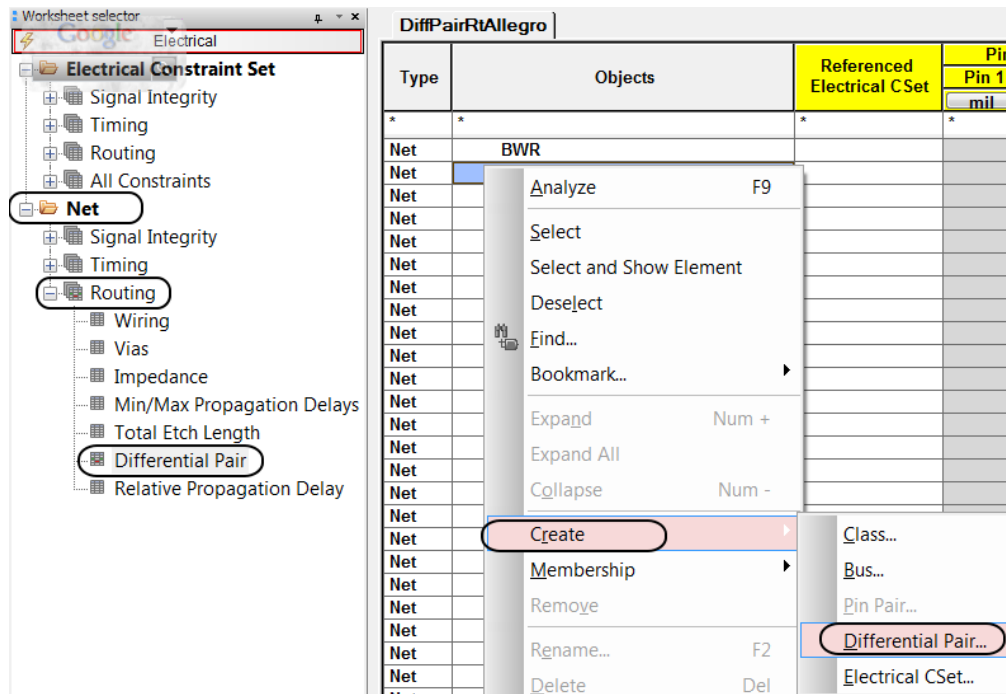
- Creating Differential Pairs in Constraint Manager
- Auto Creation of Differential Pairs

Creating Differential Pairs in Constraint Manager

To create a differential pair in Constraint Manager, do the following:

1. Open the *Net > Routing > Differential Pair* worksheet.
2. Right-click on the Net/Xnet object.
3. Select **Create > Differential Pair** from the pop-up menu.

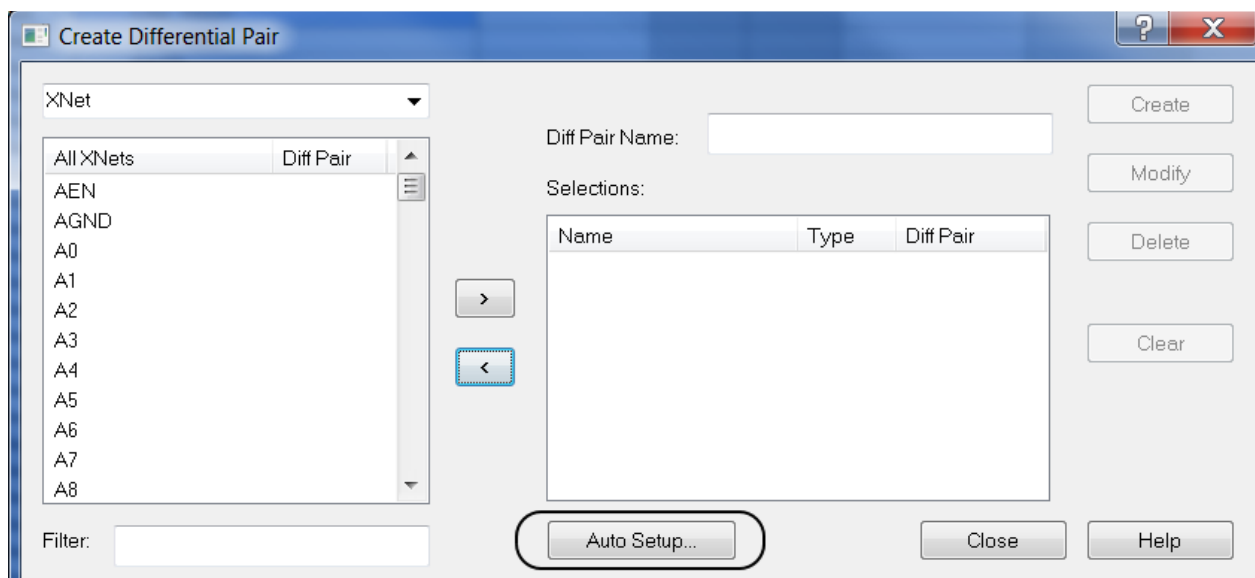
Using Differential Pairs in Allegro PCB Editor



Auto Creation of Differential Pairs

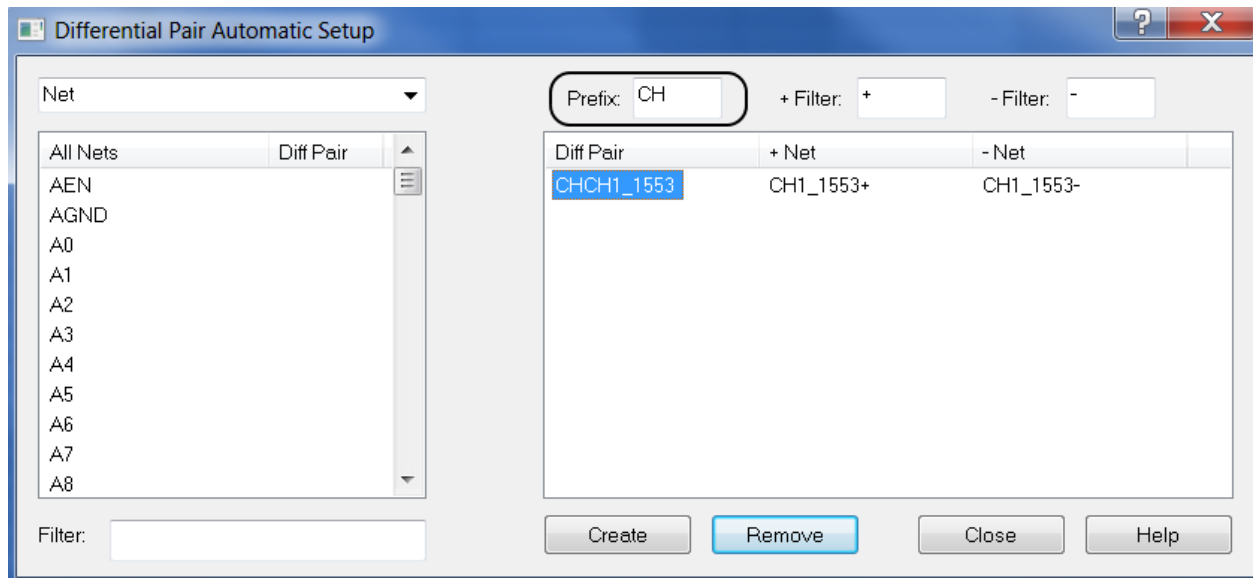
Differential pairs can be created automatically using net names. Perform the following steps for auto-creation of differential pairs:

1. In the *Net > Routing > Differential Pair* of Constraint Manager, select **Objects > Create > Differential Pair**.
2. In the Create Differential pair dialog, click **Auto Setup**.



Using Differential Pairs in Allegro PCB Editor

The *Differential Pair Automatic Setup* form opens..



Use this form to create differential pairs based on specific prefixes and filters. For example, if the net names that form differential pairs are CH1_1553+ and CH1_1553-, you can set the value of *Prefix* as *CH*, *+ Filter* as "+", and *- Filter* as "-". This settings will display all the nets that begin with *CH* and end with "+" or "-".

3. Select **Create** to create the differential pairs automatically.

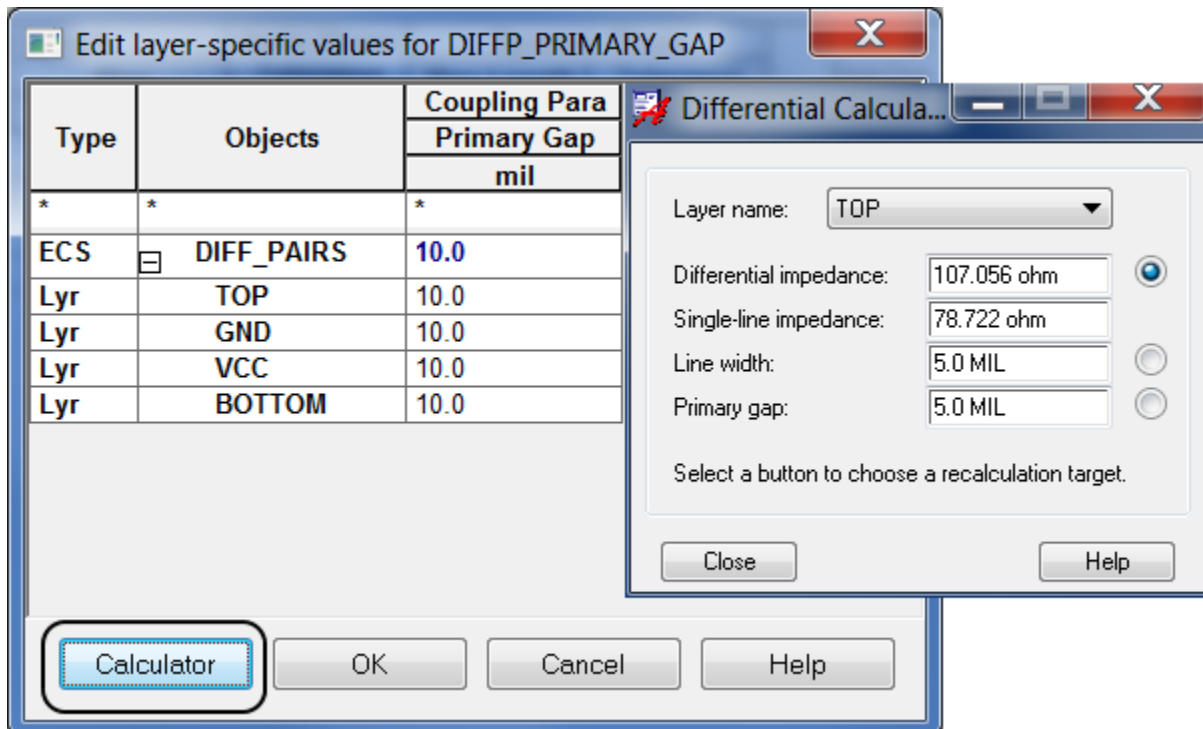
Differential Pair Calculator

The Differential Pair Calculator is used to perform what-if analysis to determine what values of Primary gap and width are needed to get specific differential and single line impedance.

The calculator is available in the Electrical Domain in Constraint Manager, from the *Electrical CSet > Routing > Differential Pair and Net > Routing > Differential Pair* worksheets.

To access the differential calculator, in the Primary Gap, Neck Gap, or +/- Tolerance cells, do the following steps:

4. Right-click and choose **Change** from the pop-up menu.
5. Select the **Calculator** button.



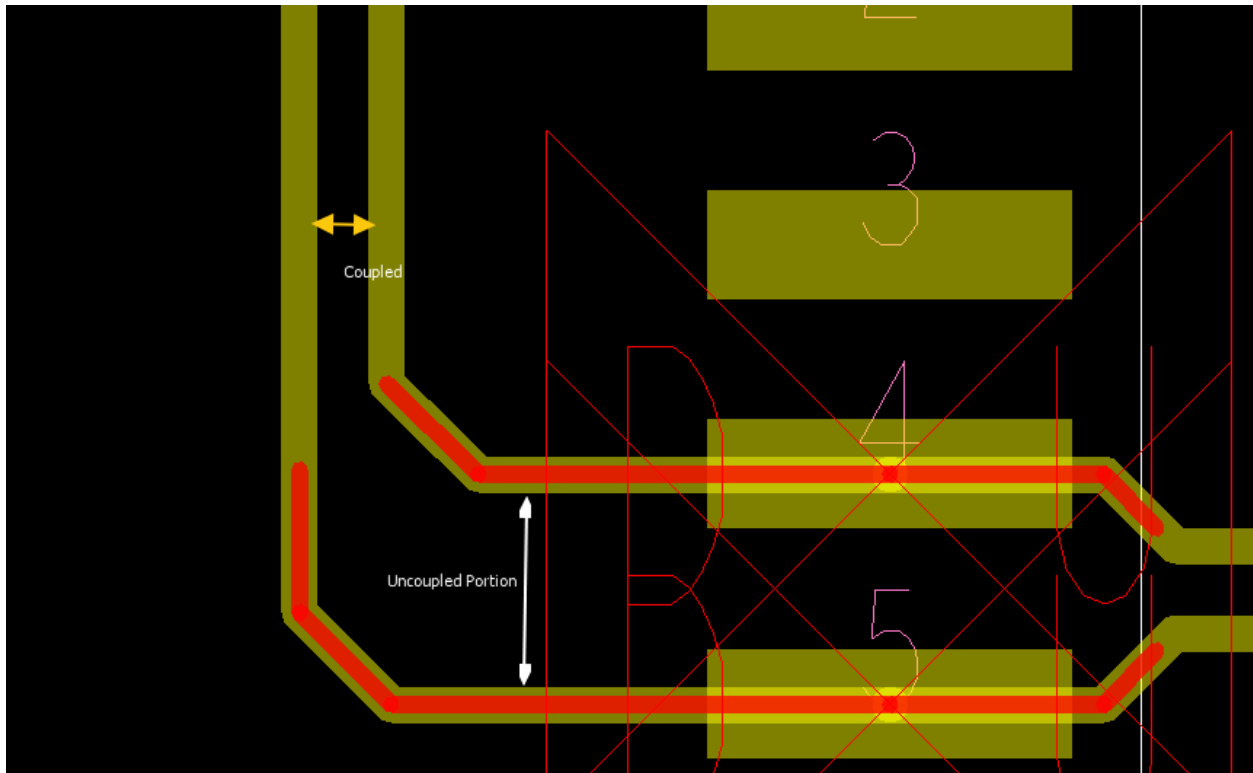
Differential Impedance in Constraint Manager

Advanced Constraints can be used to view the Differential Impedance in Constraint Manager.

A pre-defined constraint called DIFF_IMPEDANCE_RULE can be set up and added to any worksheet. The constraint is added to the *Net > Routing > Impedance* worksheet. You can add this constraint to any worksheet, or even add a new worksheet. For more information on customizing worksheets, refer to the section *Customizing Worksheets* in Allegro Constraint Manager User Guide.

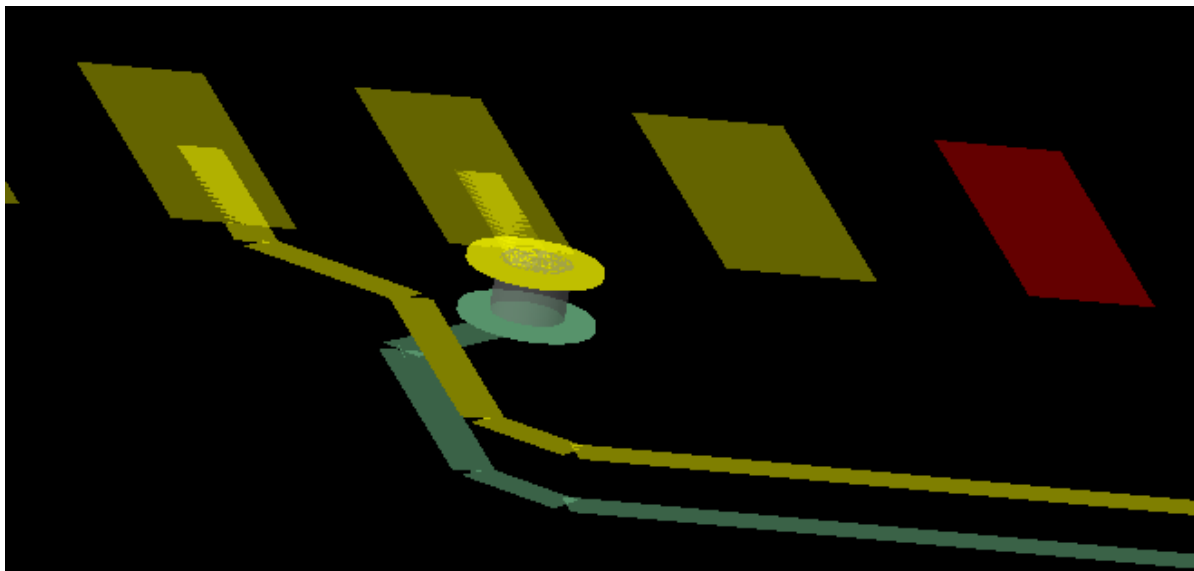
Max Uncoupled Length

The maximum length for which the two nets of differential pair can run uncoupled is constrained by the constraint, MAX_UNCOUPLED_LENGTH. This constraint is available in the *Differential pair* worksheet. If the two nets of the differential pair do not follow the gap constraints for certain length which is more than the MAX_UNCOUPLED_LENGTH constraint, the uncoupled length DRC is shown as D-U, and the uncoupled segments are highlighted as displayed in the following image:



Tandem Routing

You might need to route the two nets of differential pair on adjacent layers. This does not happen automatically in Allegro PCB Editor or Router. However, it is possible to tandem route differential pairs manually.



When routing the differential pair on different layers, the rules you set in Constraint Manager will not have any effect.

To route a differential pair on tandem layers, perform the following steps: This procedure assumes that routing will be done on the top layer and layer 2.

1. Pick the first net, for example Net1 of the differential pair for routing.
2. Right-click and select **Single Trace Mode from the pop-up menu.**
3. Route the single trace just a small segment on the top layer, click to add a corner, and right-click and select **Done.**
4. Select the second, net of the differential pair, and sw, Net2 for example, at the route layer with layer 2,
5. Route Net2 to where you ended Net1 of the differential pair and add a corner to coincide with the net on the top layer
6. Right-click and select **Done.**

You will now have the segment on the top layer for Net1 and the segment for Net2 on layer 2 exactly on top of each other.

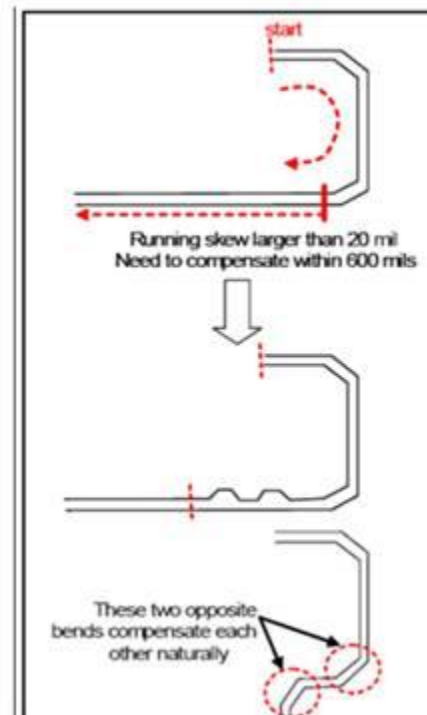
7. Select Net1 or Net2, right-click and uncheck **Single Trace Mode.**
The differential pair will now route together. To complete the routing, use the same method that was used to start the tandem routing.

Dynamic Phase Control for Differential Pairs

Differential pair technology has evolved where more stringent checking is required in the area of phase control. This is evident on higher data rates associated with parallel buses such as QPI, SMI, PCI Gen 2, DDR, QDR and Infiniband. In the simplest of terms, differential pair technology is sending opposite and equal signals down a pair of traces. Keeping these opposite signals in phase is essential ensures that they function as intended. As the current Static Phase is limited to a one time check across the entire Driver-Receiver path, a new Dynamic Phase check was introduced in SPB 16.3 that performs phase checks at bend point intervals across the differential pair.

The Dynamic Phase check is designed to meet the guidelines suggesting that the path lengths of the true and complement signals within the differential pair must differ by no more than "x mils" along the entire path of the net. If at any point on the net, the skew between true and complement exceeds "x mils", the mismatch needs to be compensated within "y mils". Representative values for x and y might be x = 20 and y = 600.

Using Differential Pairs in Allegro PCB Editor



The constraints associated with Differential Pairs now support Static and Dynamic Phase. The margins of each constraint can be set independently using length or time. The *Max_Length* (running skew) constraint for Dynamic Phase is limited to length only.

Uncoupled Length		Static Phase Tolerance	Dynamic Phase		Min Line Spacing	Primary Gap	Primary Width
Gather Control	Max		Max Length	Tolerance			
	mil	mil	mil	mil	mil	mil	mil
*	*	*	*	*	*	*	*
					0.00	0.00	5.00
Include	300.00	5 mil	600.00	20 mil	5.90	6.00	6.00

Static Phase Tolerance - A onetime check from Driver to Receiver for comparing lengths or delay of each member. If a Driver cannot be determined, the check is performed across the longest path of the pair. (No change in behavior in 16.3)

Dynamic Phase - Etch length of each member is compared at each bend point interval across the Driver-Receiver path of the Differential Pair. Etch length is always measured back to the Driver pins.

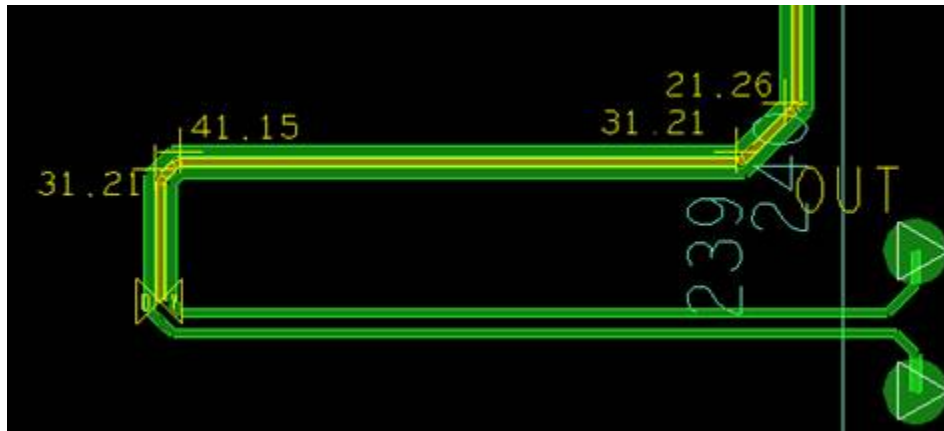
Dynamic Phase Max Length - When specified, the Differential Pair is permitted to exceed the phase tolerance constraint for a contiguous etch length of less than or equal to the value of the specified Max Length constraint. If no compensation is made within this specified distance, a DRC is reported at the point where the Differential Pair first goes out of phase.

Using Differential Pairs in Allegro PCB Editor

Let's consider an example. Assume that the Dynamic Phase constraints are set as follows:

Static Phase Tolerance	Dynamic Phase	
	Max Length	Tolerance
mil	mil	mil
*	*	*
		0.1
20 mil	300.00	20 mil

When the DRC is updated, it shows the following:



The beginning of the yellow pseudo line (closest to driver) is where the Differential Pair initially goes out of Phase (beyond the 20 mil tolerance). The DRC marker *D-Y* is placed at the initial 'out of phase spec' location as measured from the Driver Pins.

Notes:

- There can only be 1 DRC marker on a differential pair, even though there may be multiple violation zones.
- It is assumed that the designer will correct the phase issues working from the Drivers to the Receivers.

Resizing a Differential Pair

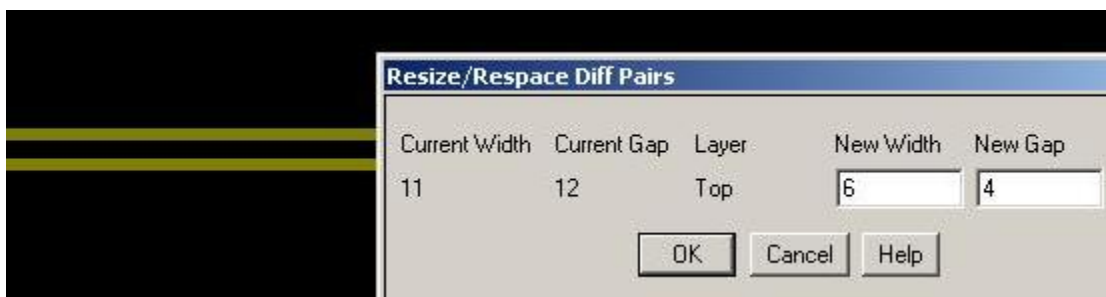
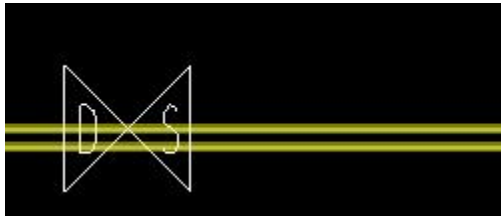
If a differential pair is already routed with specified gap, is there a way to change the Differential pair spacing?

Using Differential Pairs in Allegro PCB Editor

Use the *unsupported* command to resize the differential pairs. This command is useful when differential pair constraint changes are required after differential pair routing is complete.

Gap changes are typically accomplished by maintaining the existing (imaginary) center-line between coupled segments. When modifying any differential pairs, neighboring elements are ignored, so DRCs are likely to appear after the command is run. Constraints are not modified, and will need to be changed to match the Resize/Respace values applied.

Note: An important step is to run the *Resize/Respace Diff Pairs* command before (and not after) changing the constraints. You should not run this command again on the same differential pairs until after having updated the constraints to match the applied Resize/Respace values. Else, the command will not recognize the modified differential pair clines accurately.



Examples

Example - Differential Pair Spacing

This example shows how to set up differential pairs in Constraint Manager so they are spaced 20 mils from other nets. Specific line-to-line spacing is maintained between objects of differential pairs.

Using Differential Pairs in Allegro PCB Editor

For maintaining a larger line-to-line spacing between differential pair objects to other nets as compared to differential pairs to differential pairs, a spacing constraint could be created and assigned.

Assume that you have a requirement that differential pairs (DP) must have 20 mils spacing between each DP object and any other non-DP net while the spacing between all non-DP nets is 5 mils.

The [example.zip](#) at support site file contains two *.brd* files. Download and open the attachments.

For reference, *dp_16_space1.brd* has constraints set up to in Constraint Manager. The board *dp_16_stripped1.brd* is the same board without the constraints. It can be used with the following detailed information to accomplish the task of 20 mil spacing between DP objects and all other non-DP nets (brief steps are listed at the top of each *.brd* file).

Procedure to follow (assuming DPs are already set up):

1. Create an ECSet which will contain the DP settings.
 - a. In the ELECTRICAL domain of Constraint Manager, select the **Electrical Constraint Set > Routing > Differential Pair** worksheet.
 - b. Right-click on the design name object and choose **Create > Electrical CSet** from the menu.
 - c. Enter a meaningful name (DP_10, for example) and click **OK**.
 - d. Enter the DP electrical constraints (you may need to click on the “+” to expand the rows).

Note: Repeat steps b-d for additional constraints with different values.

2. Assign the ECSet to the appropriate DPs.
 - a. In the ELECTRICAL domain of Constraint Manager, select the **Net > Routing > Differential Pair** worksheet.
 - b. Click in the **Referenced Electrical CSet** column for the DP row(s) and select the **DP_10** ECSet from the pull-down.

Constraint Values Used:

```
=====
ELECTRICAL Domain
DP_10 ECS
3.0 Min Line Spacing (must be set
to avoid L-L DRCs of the DP)
10.0 Primary Gap
8.0 Primary Width
4.0 Neck Gap
4.0 Neck Width
1.0 (+) Tolerance
1.0 (-) Tolerance
SPACING Domain
DEFAULT SCS
5.0 All Constraints
DP_SP SCS
20.0 Line to Line
5.0 Remaining constraints
```

Using Differential Pairs in Allegro PCB Editor

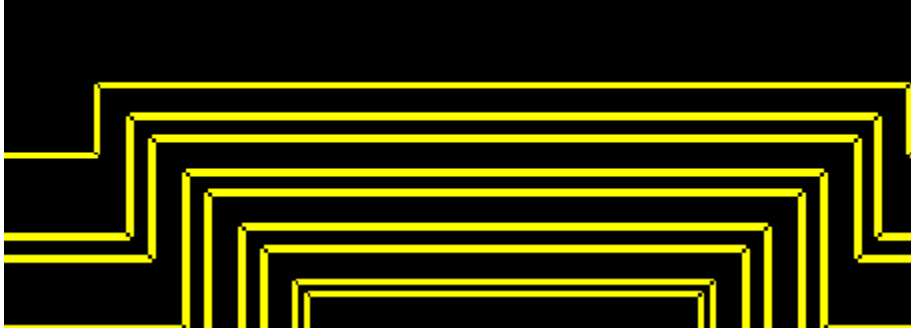
The screenshot shows the Allegro Constraint Manager interface. On the left, the 'Electrical Constraint Set' is expanded to show 'Routing' and 'Differential Pair'. The main window displays a table for the design 'dp_16_stripped1'.

Type	Objects	Referenced Electrical CSet
*	*	*
Dsn	dp_16_stripped1	
DPr	DP1	DP_10
Net	D1	DP_10
Net	D2	DP_10
DPr	DP2	DP_10
Net	D3	DP_10
Net	D4	DP_10
DPr	DP3	DP_10
Net	D5	DP_10
Net	D6	DP_10
Net	D7	
Net	D8	
Net	D9	

3. Create a Spacing Constraint Set (SCSet) with specific spacing rules for the DPs.
 - a. In the SPACING domain of Constraint Manager, select the **Spacing Constraint Set > All or By Layer(s)** worksheet.
 - b. Right-click on the design name in the Objects column and select **Create > Spacing Set**.
 - c. Enter a meaningful name (DP_SP) and click **OK**.
 - d. Enter the required DP line-to-line spacing constraint for the SCSet.
4. Create a Net Spacing Class (NCLs) and assign all DPs to the same class.
 - a. In the SPACING domain of Constraint Manager, select the **Net > All Layers** worksheet
 - b. Under the **Objects** column, select all DP objects.
 - c. Right-click on one of the selected objects and choose **Create > Net Class**.
 - d. Enter a meaningful name (DP_CLASS) and click **OK**.
5. Assign the SCSet from step 3 to the NCLs.
 - a. In the SPACING domain of Constraint Manager, select the **Net > All Layers** worksheet.
 - b. Select the **Referenced Spacing CSet** cell for the NCLs row and select the SCSet that was created in step 3 above.

Testing

Use the *slide* command to experiment with the end results. If the board is set up properly, you will be able to slide the non-DP segments upward into the others and observe the different spacings between objects.



Note: When sliding clines ensure that the *Bubble* mode is properly set in the *Options* pane.

Troubleshooting

Issue #1: Some Differential Pair Nets Do Not Slide Together

I have many differential pairs set up with three components assigned to the nets. Some parts of the pairs will slide in tandem as expected while others will not slide together.

The pin pair matching function for differential pairs gathers as much data as possible on the nets (including component class and pinuse information), to try and determine the correct set of pins to match. If a coherent set of driver/receiver pins can be determined, side branches of the net are included too, but if the data is ambiguous (no explicit driver/receiver pins), the matching code falls back on the longest path which does not include the side branch.

This can be determined by selecting *Show Element* on the clines that are not sliding as a pair. If the differential pair constraint information is not shown in the Show Element window, that branch is NOT considered.

For the branch to be considered, the Show Element window should show diffpair constraint information similar to:

Constraint information:

(DPTol) R2.1 to U1.13 min= 1272.43 MIL max= 1472.43 MIL actual= 1343.12 MIL
DPData: gap=8.00 (--0.01 +0.00) tolerance= 100.00; max uncoupled= -0.01

Note: If the *Find Filter* is set to *Nets* instead of *Clines*, all branches of the net should show the differential pair constraint information to consider the entire net. If all branches of the net do not show differential pair constraint information, the missing branches will NOT be considered a pair and slide together.

Solution:

Change the pinuse of the pins on the net so there are explicit driver (OUT)/receiver (IN) pin pairs on the differential pairnets.

To change the pinuse on the pins:

1. Choose **Edit > Property**.
2. Under the Find tab, select only **Pins**.
3. Select all the pins in the net.
4. In the Edit Property form, select **Pinuse** and change to the appropriate pinuse.

Note:

A DRIVER pin is a pin with a pinuse of OUT, TRI, OCA or OCL

A RECEIVER pin is a pin with a PINUSE of IN

Example of pinuse on a net that will NOT consider the entire net a differential pair:

Pin	Type
U1.12	TRI
C1.1	OUT
R1.1	OUT

Example of pinuse on a net that WILL consider the entire net a differential pair:

Pin	Type
U1.14	TRI
C3.1	IN
R3.1	IN

Issue #2: How to Remove Electrical Differential Pair Objects from Constraint Manager

I have deleted all differential pair properties from all the nets in my design, but some differential pair objects still show up in Constraint Manager. A right-click action on the differential pair in Constraint Manager displays a pop-up menu where I would usually delete the differential pair, but the *Delete* command is grayed out. How do I delete these differential pair objects?

Solution:

These differential pairs may have been electrically (or automatically) defined by a component's signal model. To remove these differential pairs, you must first determine the signal model that defines the differential pair and remove the differential pair definition from the signal model.

To find the SIGNAL_MODEL

1. Right-click on the differential pair.

The differential pair is highlighted in Allegro PCB Editor.

2. Choose **Display > Element** (Find Filter set to **Comps** only).
3. Select a pin of each component that is connected to the differential pair.
4. Look for the **SIGNAL_MODEL** property assigned to a component.

To remove the differential pair definition from the SIGNAL_MODEL

Using Differential Pairs in Allegro PCB Editor

1. Choose **Analyze > SI/EMI Sim > Model**.
2. If a window about DC nets pops up and prompts you to continue, select **Yes**.
3. In the Signal Model Assignment form, select the device in the form or the component in the canvas
4. Select **Edit Model**.

If the differential pair is electrically defined, the right hand column will show DiffPair Mate pins next to the Wire column.

5. Select one of the two pins. The IBIS Device Pin Data form will open.
6. Under the Differential Pair Mate Type, select the pull-down arrow and choose **None**.
7. Select **OK**.
8. If additional differential pairs are defined on the model, select another pin from the DiffPair Mate column and repeat steps 5-7.
9. Select **OK** in the IBIS Device Model Editor form. The differential pairs will now be removed from Constraint Manager.