

Differential Pairs – Supplemental Notes.

Differential Line Spacing

The Primary Gap is the edge-to-edge gap at which your differential pairs will be routed. You can also define a positive and negative tolerance to this primary gap. If the gap between the differential pair is within the positive and negative tolerance of the primary gap, then the nets are considered coupled at that point. If the gap of the differential pair is outside of the tolerance of the primary gap, then the primary gap, then the pair is uncoupled.

If the amount of uncoupled routing is greater than the maximum uncoupled length constraint, then a DRC will be generated. If the gap between the pairs is less than the minimum line spacing at a point on the nets, then a DRC error will automatically be generated.

Coupled Tolerance

Coupled tolerance is generally used to account for bends in the routing of the differential pairs. When differential pairs are routed in the Allegro/OrCAD PCB Editor, the gap as the pair bends cannot maintain the exact primary gap because of geometric issues. Assigning a small positive and negative tolerance to the primary gap allows for these insignificant variations in the primary gap, while allowing the differential pairs to still be considered coupled.



Uncoupled Length

The nets of a differential pair are considered uncoupled when the edge-to-edge gap between the pair is not within the positive and negative tolerance of the primary gap. If the sum of all the uncoupled length of either net in the pair is greater than the maximum uncoupled length constraint, then a constraint error is flagged. The maximum uncoupled length constraint is used to account for the entering and exiting of pins, as well as for breaking the primary gap to avoid other routing obstacles such as vias (but this is normally not done). As with all other constraints, the maximum uncoupled length constraint violations will be flagged in both Constraint Manager and the Allegro/OrCAD PCB Editor. When you view the constraint violation in Allegro/OrCAD PCB Editor, you will also notice that the uncoupled portions of the differential pair are displayed in the same colour as the DRC marker.

Gather Control

You can set the Gather Control constraint to either **Include** or **Ignore.** The default is **Include**, which means that any uncoupled length required by the exit or entrance of the pins will be included in the calculation of the total

uncoupled length. If you set the Gather Control constraint to **Ignore**, then the uncoupled length needed to enter or exit pins will not be included in the calculation of the total uncoupled length.

Static Phase Tolerance

The phase tolerance is used to assure that the length or delay of the nets in a differential pair is within a userdefined constraint. You can set a phase tolerance in either length units or time units (license dependant), but the length of the two nets in the pair must be matched with that tolerance or a constraint violation with be flagged. The phase tolerance is used to accommodate physical issues in a board layout that would prevent two nets in a pair from being routed at exactly the same length. These issues can include placement issues or issues regarding routing blockages in the design.

Or a simpler definition can be a onetime check from Driver to Receiver comparing lengths or delay of each member. If a Driver cannot be determined, the check is performed across the longest path of the pair.

Dynamic Phase Control (license dependant)

Static phase control is useful for preventing the skewing of nets within a differential pair by maintaining similar propagation delays within the pair but another benefits of using differential pairs is noise immunity on the pair. Any external noise applied to the pair is applied equally to both mates and is effectively cancelled out. Static phase control only checks the completed length of the net. If the nets are out of phase for the majority of the connection and then brought back into phase at the end this will not be checked by the static phase control and noise immunity may be compromised. Dynamic phase control allows you to verify that the mates of a differential pair are within tolerance along the entire length of the pair. If the length of the pair goes out of tolerance, it must be compensated within the Max Length or a design constraint will be created.

Or a simpler definition can be etch length of each member is compared at each bend point interval across the Driver-Receiver path of the Diff Pair. Etch length is always measured back to the Driver pins.

Dynamic Phase Max Length

When specified, the Diff Pair is permitted to exceed the phase tolerance constraint for a contiguous etch length of less than or equal to the value of Max Length specified. If no compensation is made within this specified distance, a DRC shall be reported at the point where the Diff Pair first goes out of phase.

Layer-Based Differential Pair Values

The constraints in the Differential Pair worksheet of the Electrical Constraint Set do not accommodate different values for different layers of the printed circuit board. Depending on the makeup of the PCB you may have different differential impedances as you traverse the different layers of the PCB. You will often need to have different line widths and gaps on the different layers of the PCB to maintain the desired differential impedance. If layer dependant lines and gaps are required for routing differential pairs, leave the physical parameters in the ECSet blank and use the physical constraints sets for line width, primary gap, and tolerance definitions. The DRC system first looks at the electrical constraints set for its values. If not populated, it then looks at the gap widths defined in the physical constraint sets.

NOTICE OF DISCLAIMER: Parallel Systems is providing this design, code, or information "as is." By providing the design, code, or information as one possible implementation of this feature, application, or standard, Parallel Systems makes no representation that this implementation is free from any claims of infringement. You are responsible for obtaining any rights you may require for your implementation. Parallel Systems expressly disclaims any warranty whatsoever with respect to the adequacy of the implementation, including but not limited to any warranties or representations that this implementation is free from claims of infringement and any implied warranties of merchantability or fitness for a particular purpose.

The following are trademarks or registered trademarks of Cadence Design Systems, Inc. 555 River Oaks Parkway, San Jose, CA 95134 Allegro[®], Cadence[®], Cadence logo[™], Concept[®], NC-Verilog[®], OrCAD[®], PSpice[®], SPECCTRA[®], Verilog[®] **Other Trademarks**

All other trademarks are the exclusive property of their prospective owners.