



Via-in-Pad Overview

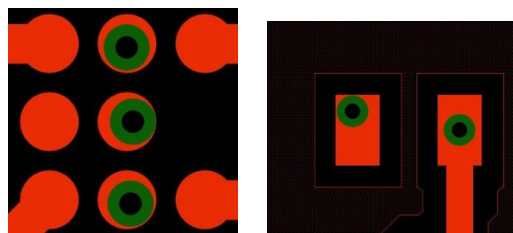
Via-in-Pad is a common fanout strategy used on HDI designs, especially on BGAs with package pitch of 0.8 mm or less. With Via-in-Pad, component placement can be more compact; capacitors can be placed closer to the device pins they need to bypass. Via-in-pad also has its drawbacks as it can introduce soldering issues in manufacturing. Solder can wick down through the open holes, if not plugged, drawing solder off the component pad. Different rules may exist for metal and soldermask defined pads. For metal defined pads, a via should be contained within the bounds of the SMD pad otherwise the solderpaste will spread out to include the via resulting in possible tomb-stoning of components. With soldermask defined pads, a via may be allowed to float within the SMD pad up to the point where the centre of the via hole intersects the edge of the SMD pad. Typically, thru-hole vias are not allowed in SMD pads. Thru-hole vias can result in solderpaste flowing down the barrel of the hole. However, capabilities must be there to allow such conditions for thermal, RF shielding and power applications.

Via-in-Pad DRC Suite

A suite of DRC checks ensures the placement of vias is properly contained within SMD pads. These checks originated in the PCB Router (Spectra) and are now fully integrated into the PCB Editor tools (OrCAD and Allegro). Via-in-Pad checks are run at the design level but override capability at the symbol level is possible with properties.

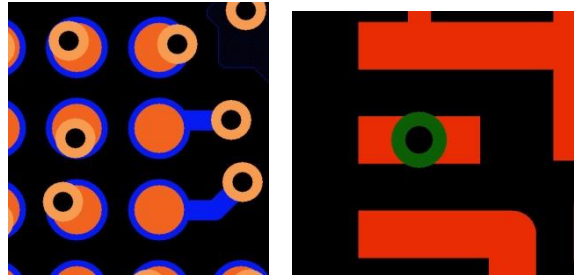
Via at SMD > Fit On

This check is designed for metal defined pad applications where vias must be totally contained within the boundary of the SMD pad. A DRC is generated if the via pad protrudes outside the SMD pad. The examples below show legal via-in-pad placement for this check condition.



Via at SMD – Fit Off

This check is designed for soldermask defined pads where a via is allowed to float outside the edge of an SMD pad up to the point where the centre of the via is still inside the SMD pad. Floating the centre of a via beyond the edge of the pad would result in acid trap formations. Other applications for this check might include vias placed in narrow SMD pads, ones typically associated with QFP devices.



Via at SMD Thru

This check is designed to detect placement of thru-hole vias within the SMD pad boundary.

Mode Settings

Mode settings for Via-in-Pad constraints are located in either Constraint Manager > Analyze > Analysis Modes > Design > SMD Pin or Setup > Constraint Modes > Design > SMD Pin (OrCAD) or Setup > Constraints > Modes > Design > SMD Pin (Allegro). The constraints align with the names used in the PCB Router.

Via at SMD Pin – ‘On’ activates the Via-in-Pad DRC Check

- **Via at SMD fit required– ‘On’** state = via pad must be contained within SMD pad
- **Via at SMD fit required– ‘Off’** state = centre of via cannot extend beyond edge of pad
- **Via at SMD thru allowed – ‘On’** state = Thru vias allowed in SMD pads
- **Via at SMD thru allowed – ‘Off’** state = Thru vias not allowed in SMD pads

Analysis Modes

	Name	Value	On	Off	Batch
	Mark All Constraints		<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
	General		<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
	Soldermask		<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
	Acute Angle Detection		<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
	Package		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
	SMD Pin		<input type="checkbox"/>	<input checked="" type="checkbox"/>	
	Via at SMD pin		<input type="checkbox"/>	<input checked="" type="checkbox"/>	
	Via at SMD fit required			<input checked="" type="checkbox"/>	
	Via at SMD thru allowed				
	Etch turn under SMD pin		<input type="checkbox"/>	<input checked="" type="checkbox"/>	
	Spacing Options				
	Mechanical Spacing		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

Property Overrides

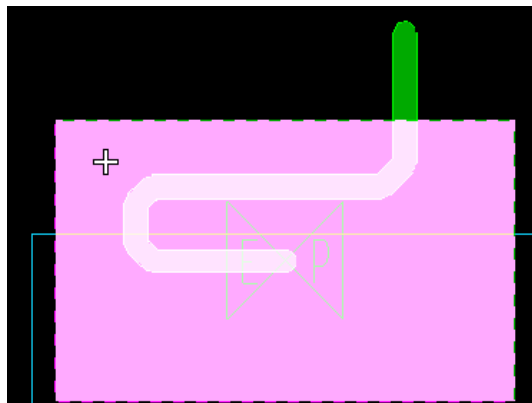
Not all packages may conform to a design level check. It may be common to use Via at SMD Pin ‘Fit on’ as a Design level check but certain packages may lend themselves to ‘Fit Off’ behaviour. Specific properties are available for the Via at SMD Pin checks that override the behaviour of the design level check. They include:

Property	Values	Apply to
Via_at_SMD_Fit	On or Off	Pin, Symbol
Via_at_SMD_Thru	True or False	Pin, Symbol

Etch Turn Under SMD Pin DRC

This check is designed to detect etch compensation buried within the pad. Driven by concern that etch segments within pad boundaries adversely affect timing rules, the checker reports if more than 2 vertex point is located within the pad boundary and by default applies to nets that have timing or length rules. A drawing level property is available to run on all nets if necessary. An exception property exists and can be applied to irrelevant nets.

Property	Values	Apply to
Etch_Turn_Under_All_Pads	True or Off	Drawing
Etch_Turn_Under_Pad_Exempt	True or Off	Net



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