



Allegro Tips and Tricks

This document provides Tips and Tricks recommended by Ed Hickey, Product Engineering Director of Cadence.

What SW version was my database saved in? (All Levels)

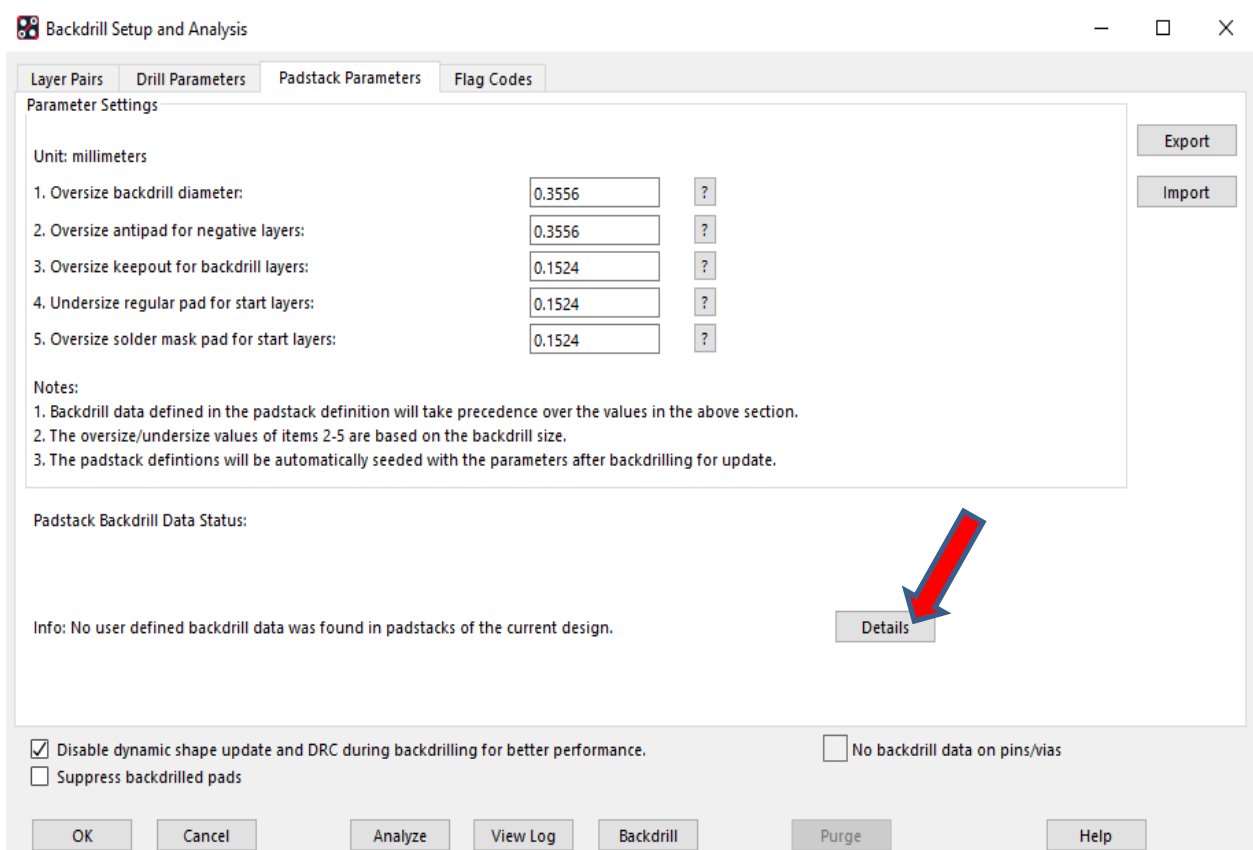
As of release 17.2 S058, the database stores the last program and release the database was saved with. Use the command dbstat -l to retrieve this information. For the near term, this option is undocumented.

Maintaining Custom Menus and Shortcuts (All Levels)

Questions related to custom menus, especially around the time of new release migration comes up often. It is recommended to go through Adding and Appending Allegro Menu Items using SKILL. Please see:- [How to customize menus and keyboard commands in PCB Editor \(parallel-systems.co.uk\)](https://parallel-systems.co.uk/how-to-customize-menus-and-keyboard-commands-in-pcb-editor) for further information.

Backdrill (OrCAD Professional and above)

Backdrill can be driven by library data or from the associated parameter form. It's important to know the library driven model will always take priority over the parameter entries. How do you know if all via and pin pads in your database have backdrill library data? Click the "Details" button as shown below for an assessment. This should be done early on to give the library folks time to make the updates.



Backdrill Setup and Analysis

Layer Pairs | Drill Parameters | Padstack Parameters | Flag Codes

Parameter Settings

Unit: millimeters

1. Oversize backdrill diameter:	0.3556	?
2. Oversize antipad for negative layers:	0.3556	?
3. Oversize keepout for backdrill layers:	0.1524	?
4. Undersize regular pad for start layers:	0.1524	?
5. Oversize solder mask pad for start layers:	0.1524	?

Notes:

1. Backdrill data defined in the padstack definition will take precedence over the values in the above section.
2. The oversize/undersize values of items 2-5 are based on the backdrill size.
3. The padstack definitions will be automatically seeded with the parameters after backdrilling for update.

Padstack Backdrill Data Status:

Info: No user defined backdrill data was found in padstacks of the current design.

Details

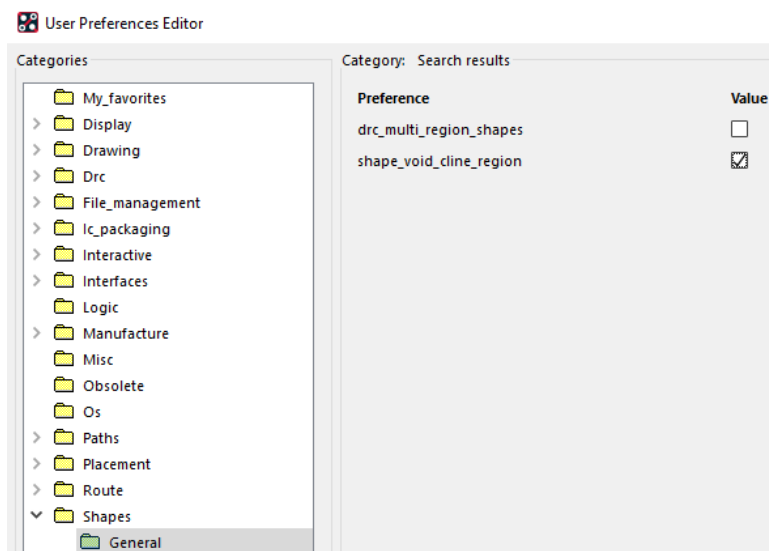
☒ Disable dynamic shape update and DRC during backdrilling for better performance. ☐ No backdrill data on pins/vias

☐ Suppress backdrilled pads

OK Cancel Analyze View Log Backdrill Purge Help

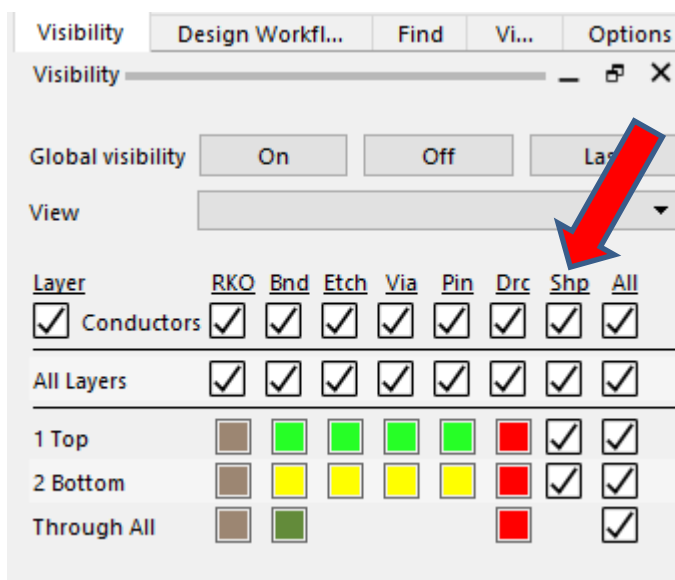
Constraint Regions – Shape Voiding (All Levels)

By default, a cline crossing a region boundary will be voided to the larger of the inside/outside constraint values. Some Customers desire what is referred to as vectorized behaviour where the line to shape spacing follows the explicit rules defined. The user preference variable “shape_void_cline_region” can be enabled to change the default behaviour.



Add Shape Header to Visibility Pane (All Levels)

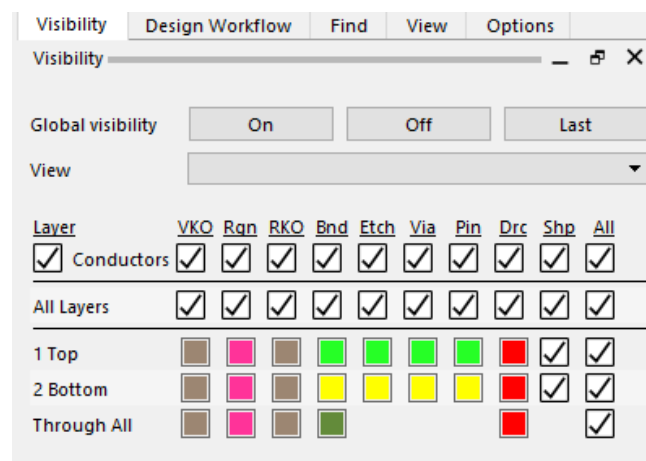
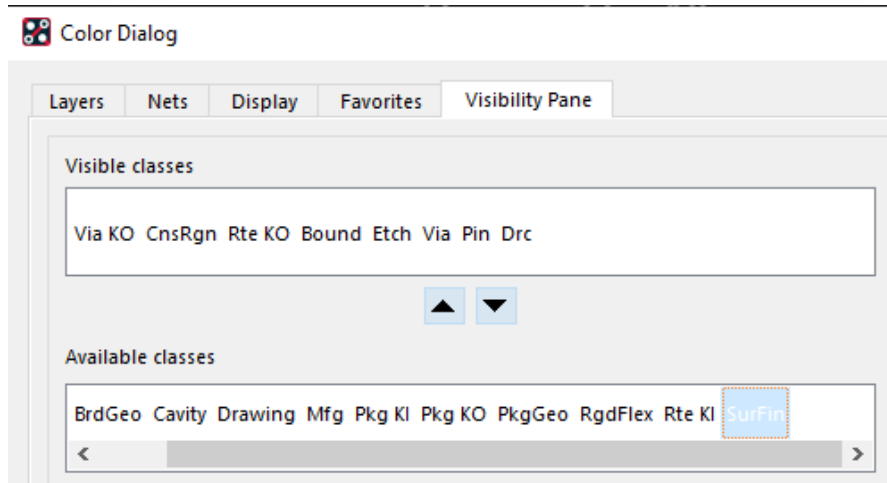
Enable the user preference variable “shape_layer_visibility_env” then restart PCB Editor. This will allow you to quickly turn on/off the visibility of shapes by layer or globally.



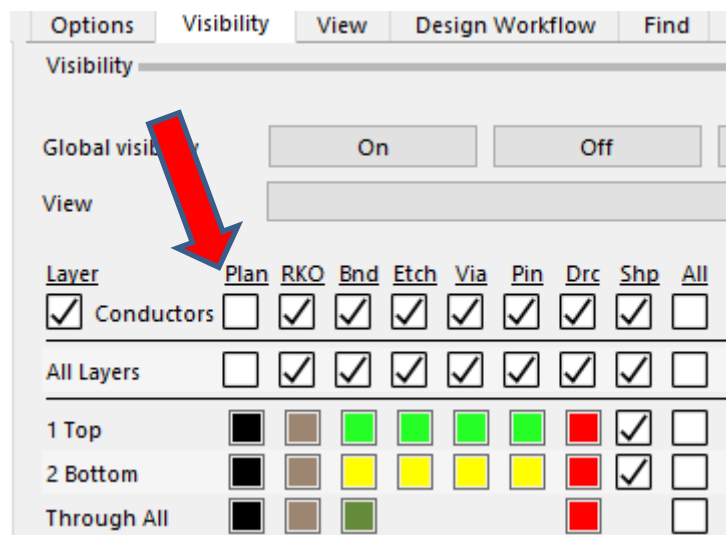
shape_in_rko_keep_shape_filled	<input type="checkbox"/>	Command	<input type="checkbox"/>
shape_layer_visibility_env	<input checked="" type="checkbox"/>	Restart	<input type="checkbox"/>

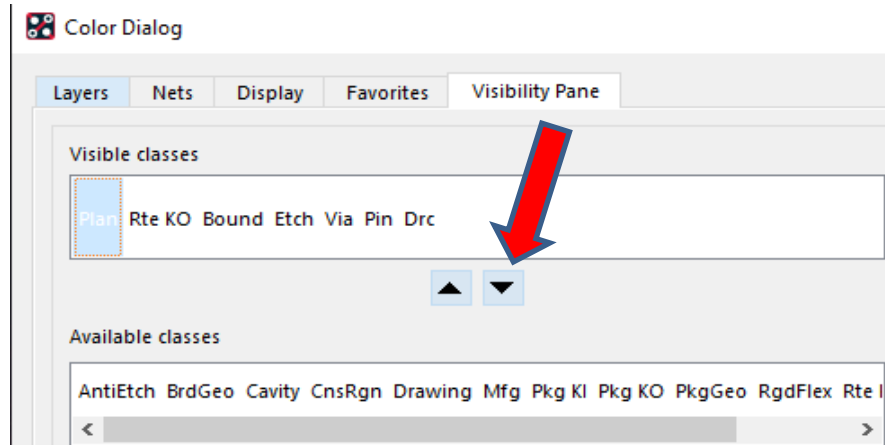
Add/Remove Classes to the Visibility Pane (All Levels)

Add your most frequented classes to the visibility pane by invoking the color dialog – Visibility Pane Tab then drag or double click from the “available classes” section. In the example below, Via KO, Route KO and Constraint Region classes were appended to the pane header. They are abbreviated to conserve space.



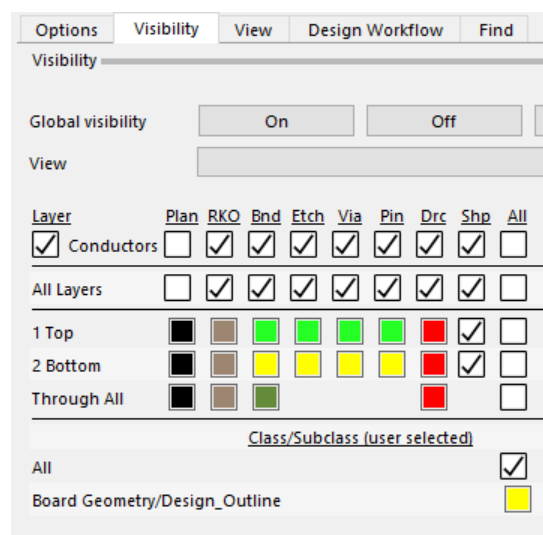
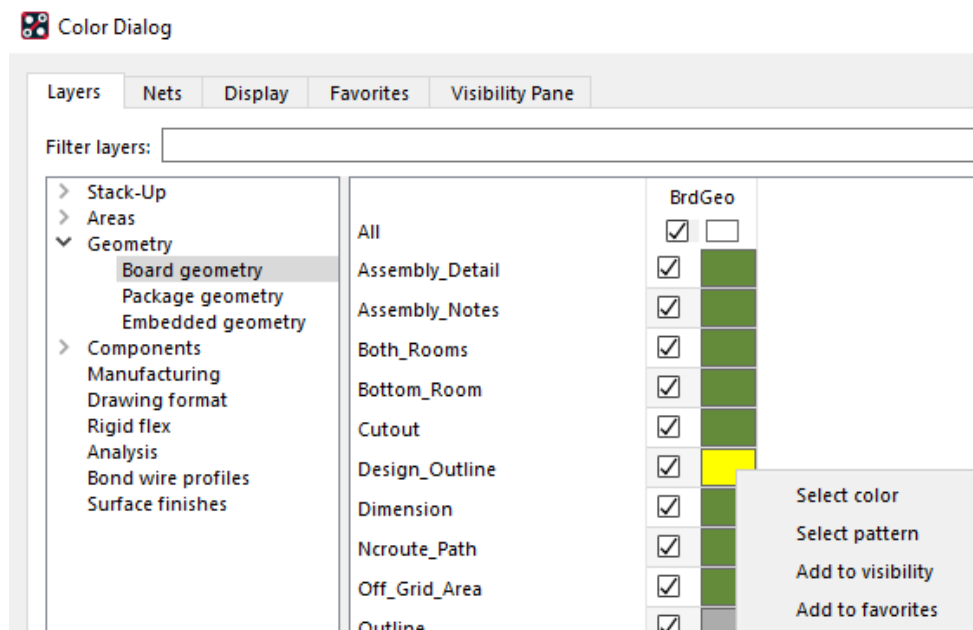
If you do not leverage the flowplan/bundle features (Allegro), you may wish to remove the “Plan” column. Following the steps provided above, select “Plan” for the “visible classes” section then click the down arrow (or double click Plan) to remove it.





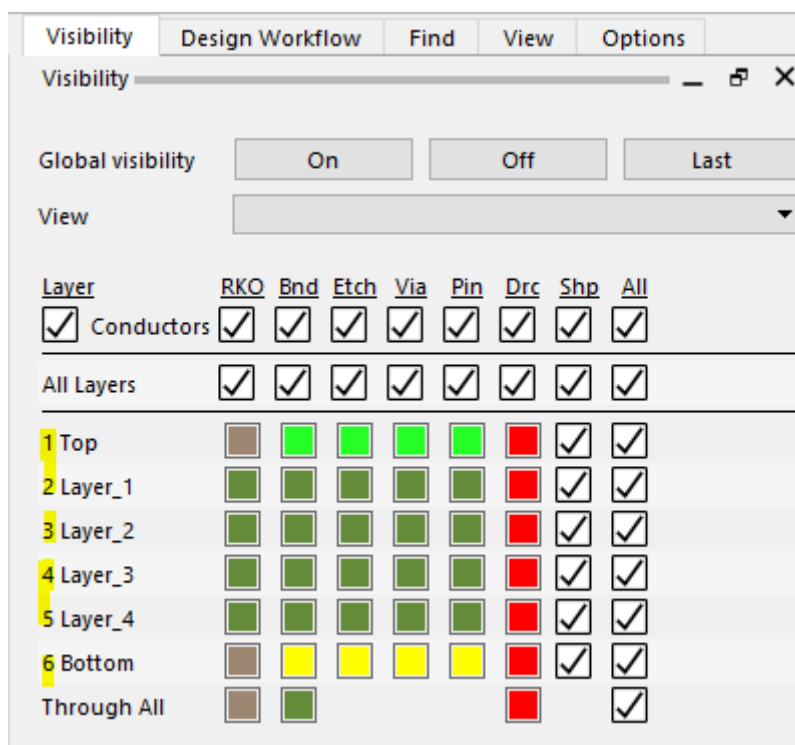
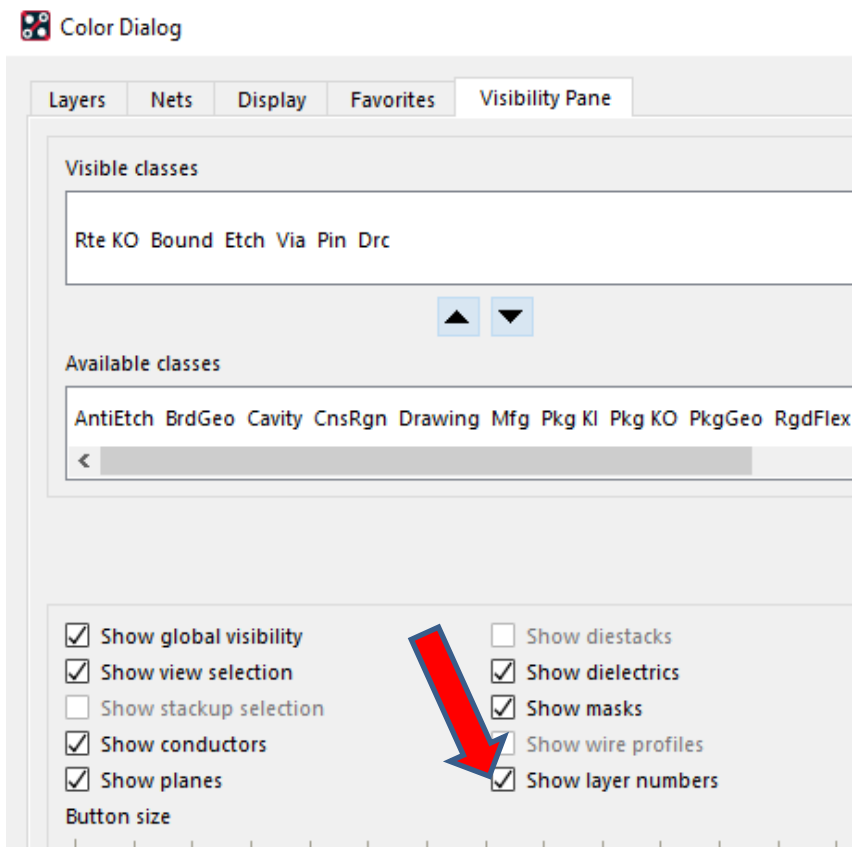
Add subclasses to the Visibility Pane (All Levels)

Add your most frequented subclasses to the visibility pane by invoking the color dialog – Layers tab. Navigate to the subclass then hover over the color swatch followed by a “right click – Add to Visibility”. In the example below, “Design Outline” is added to the Class/Subclass section of the pane.




Display Layer Numerical Sequence in Visibility Pane (All Levels)

If you are having difficulty mapping via labels to actual layer names or simply wish to see a numerical order to the stackup, consider enabling the “show layer numbers” option in the color dialog. When set, the sequential layer numbers appear in the first column of the visibility pane.

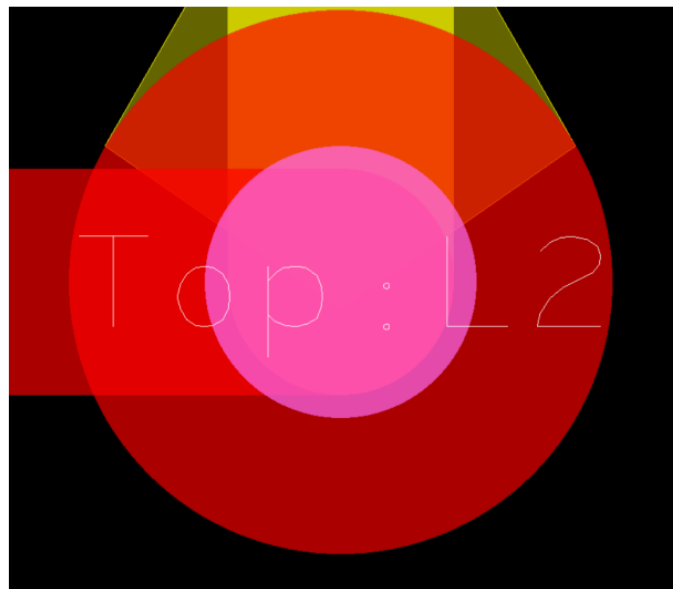


Customizing Via Labels

By default, the values associated with BB via labels begin with 1 (layer top) and increase sequentially. This may cause confusion as labels may be out of sync with the actual layer names. Consider editing the Layer ID field associated with the Cross Section Editor. There is a max 3-character limit.



Objects		Types		Thickness	Physical	
#	Name	Layer	Layer Function	Value mm	Layer ID	Material
*	*	*	*	*	*	*
		Surface				
1	TOP	Conductor	Conductor	0.03048	TOP	Copper
		Dielectric	Dielectric	0.2032		Fr-4
2	LAYER_1	Conductor	Conductor	0.03048	L2	Copper
		Dielectric	Dielectric	0.2032		Fr-4
3	LAYER_2	Conductor	Conductor	0.03048	L3	Copper
		Dielectric	Dielectric	0.2032		Fr-4
4	LAYER_3	Conductor	Conductor	0.03048	L4	Copper
		Dielectric	Dielectric	0.2032		Fr-4
5	LAYER_4	Conductor	Conductor	0.03048	L5	Copper
		Dielectric	Dielectric	0.2032		Fr-4
6	BOTTOM	Conductor	Conductor	0.03048	BTM	Copper
		Surface				



Shape Boundary Editing (All Levels)

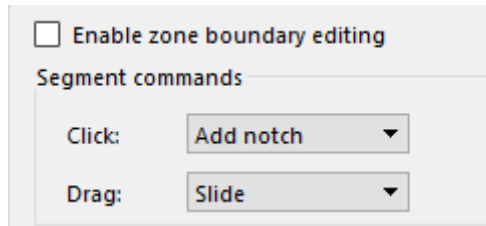
If you are not already using the Shape Application Mode to edit shape boundaries, this section is a must read! The app mode is designed to improve your efficiency in the following areas:

- Slide shape edges with or without corners
- Corner conversions to round or chamfer

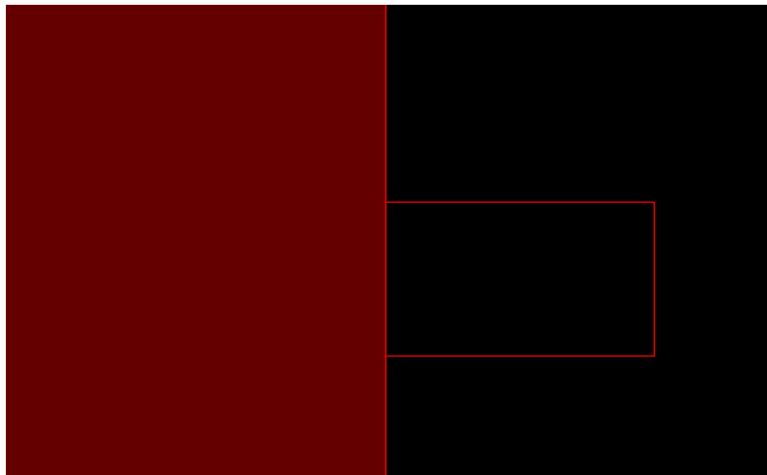
- Multi-segment sliding
- Adding of notches

Steps:

1. Enable the app mode! Setup – Application Modes – Shape Edit
2. Find filter adjustment – recommend all elements are enabled, especially shapes.
3. Choose Left click and drag behaviour.



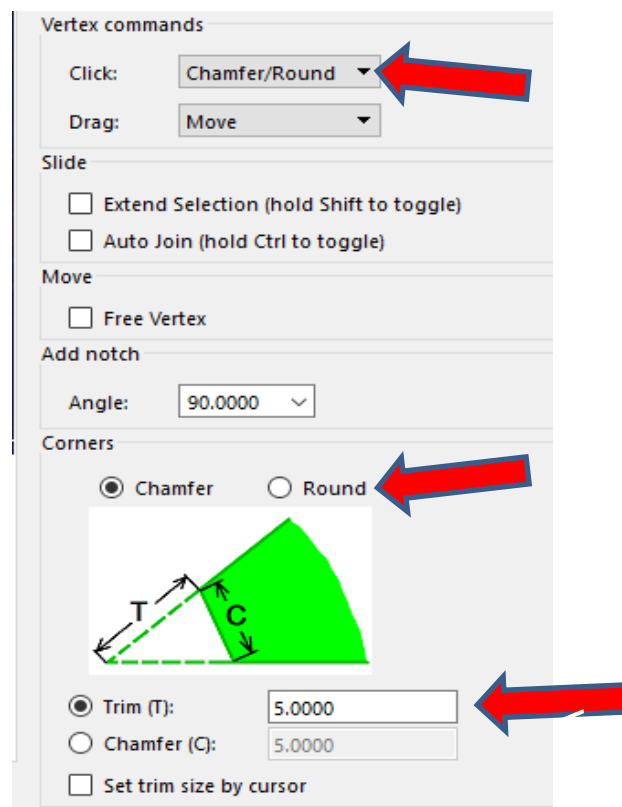
4. Add a notch by making 2 clicks on the shape boundary.



5. Slide an edge by holding the LMB button then drag.



6. Convert an orthogonal corner by clicking the vertex location; adjust settings for chamfer or round. Note the cursor changes appearance when hovering over corner.

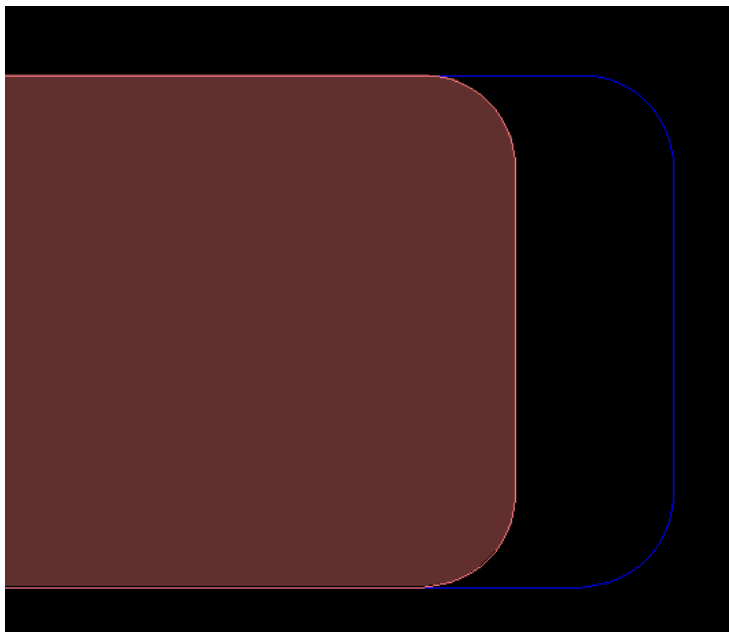
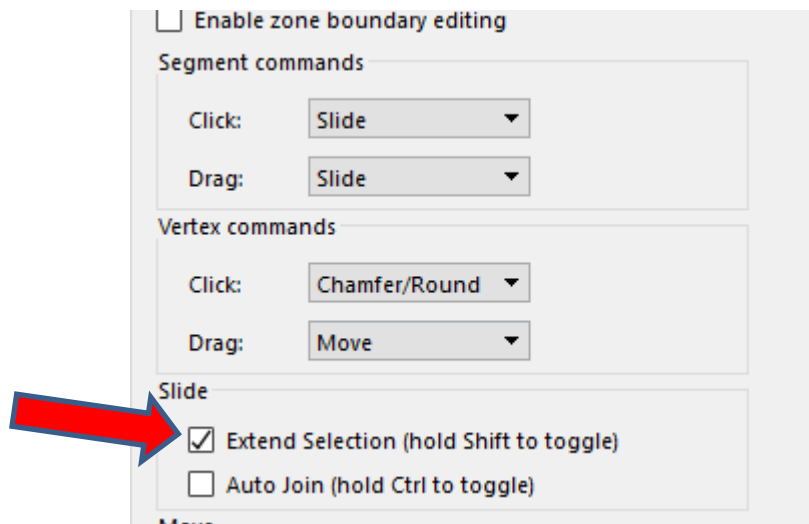


7. Most common question – how do I convert all corners? Hover over shape then use right click to access the “Trim Corners” command.





8. Second most common question – how do I slide an edge with round or chamfered corners? Enable the “Extend Selection” option then use left click drag to slide the edge with its associated corners.



9. Convert chamfered/rounded corner to orthogonal - adjust the “Click” option to “Remove/Extend”. Select a rounded corner to revert to Orthogonal.

☐ Enable zone boundary editing

Segment commands

Click: Remove/Extend ▼

Drag: Slide ▼

Vertex commands

Click: Chamfer/Round ▼

Drag: Move ▼



Voids under SMD Pads (All Levels)

The padstack supports an Adjacent Layer Keepout field that can be used for this application or even drill overshoot. Generally, the librarian controls the adjacent layer geometry in the pad definition while the Designer adds the layer depth control via the following properties.

Properties:

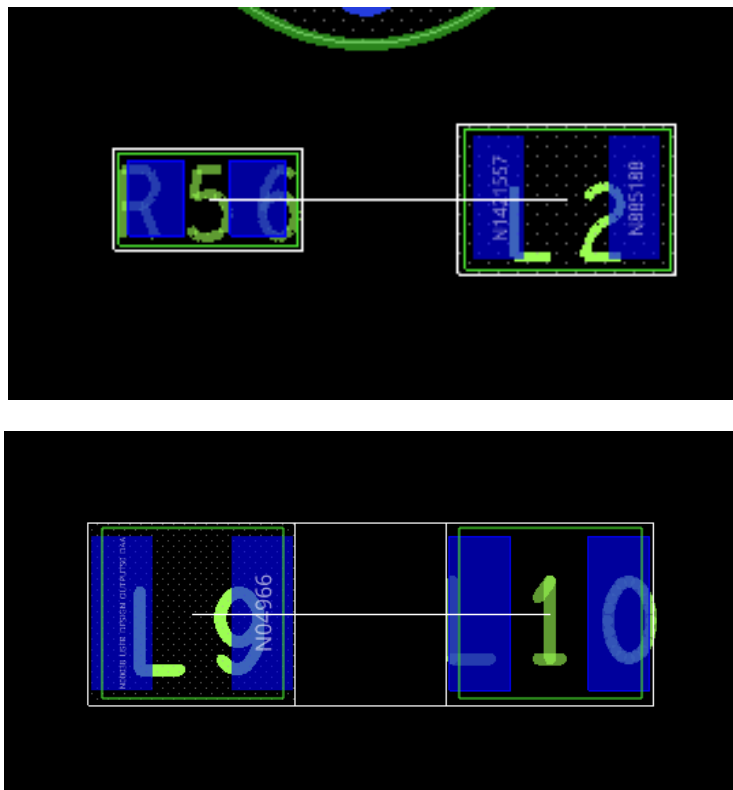
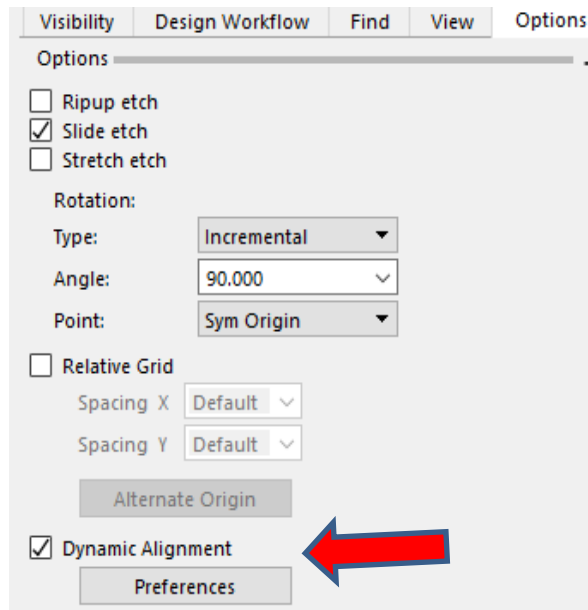
- Adjacent_Layer_Keepout_Above
- Adjacent_Layer_Keepout_Below
- Max adjacent layer count = 8

Benefit: The keepout are associated with the symbol therefore move with it!

Start	Drill	Secondary Drill	Drill Symbol	Drill Offset	Design Layers	Mask Layers
Select pad to change						
	Layer Name	Regular Pad	Thermal Pad	Anti Pad	Keep Out	
	BEGIN LAYER ▼	Rectangle 2.5000x1.5000	None	None	None	
	ADJACENT LAYER	-	-	-	Rectangle 3.0000x2.0000	

Component Placement - Dynamic Alignment (All Levels)

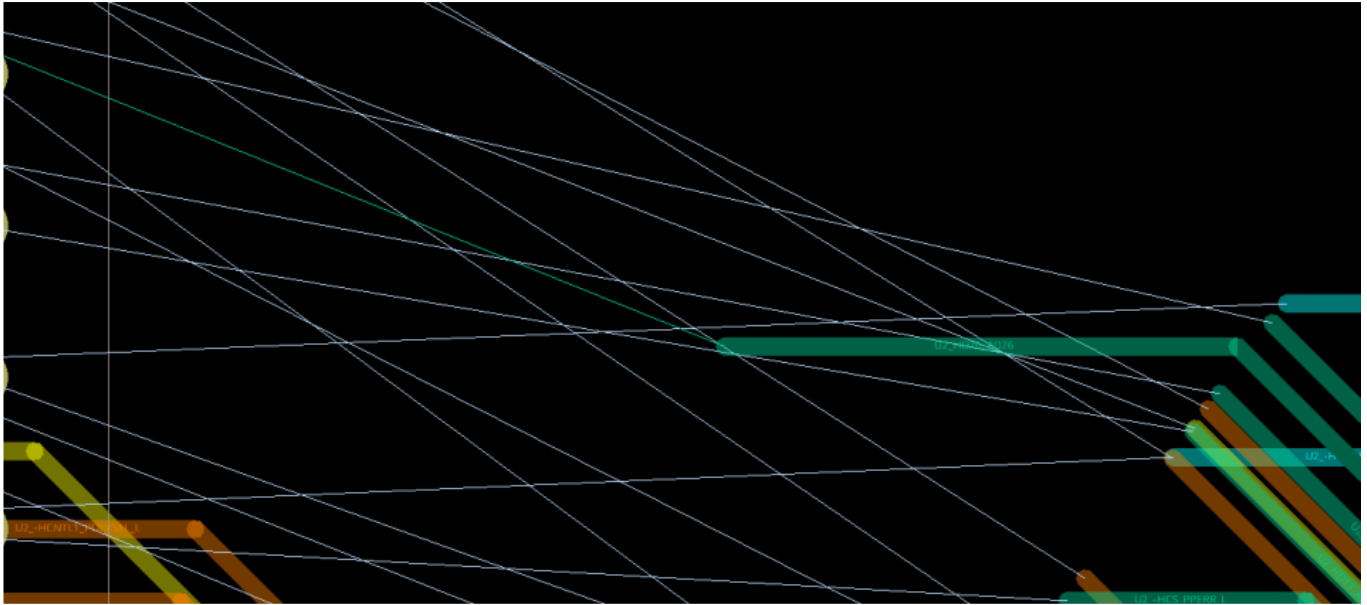
Consider enabling the Move command option “Dynamic Alignment”. When set, symbols can be aligned by its origin or Place_Bound shape edge.



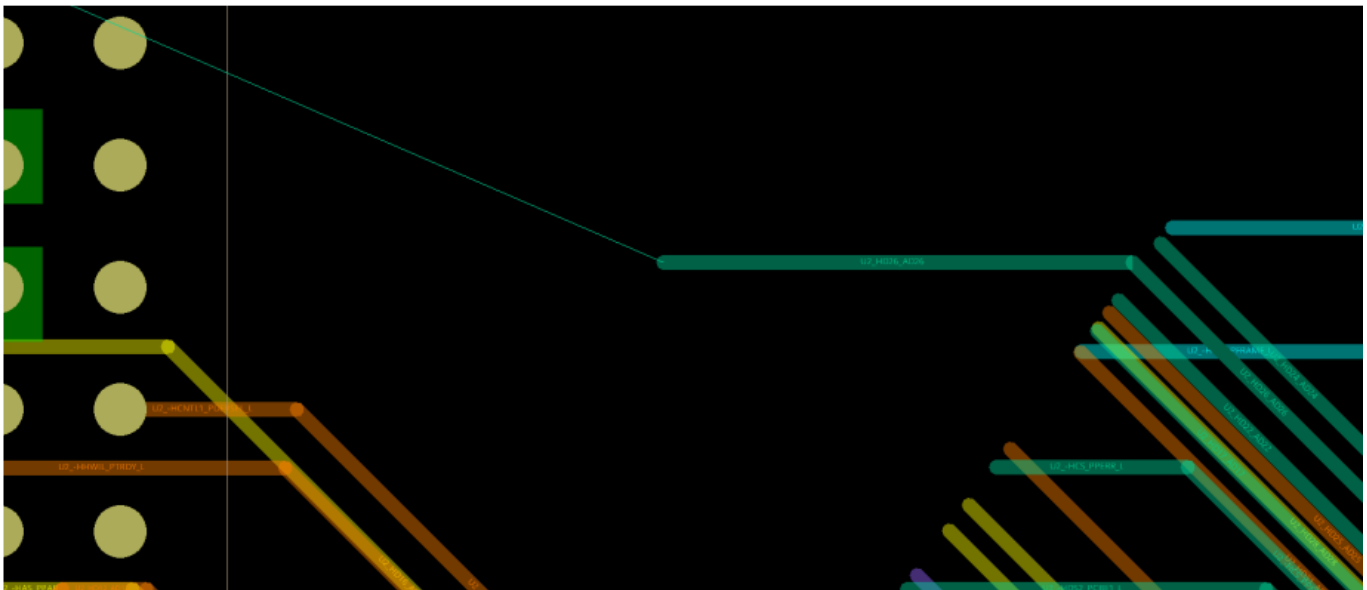
Customize the color of the alignment guides by accessing the color dialog – display folder.

Routing - Dynamic Rat Suppression (All Levels)

When in the Add Connect command, consider enabling the option “auto-blank other rats”. The image below shows a cluster of rats, most likely denser conditions exist on your board design.



With the auto-blank option enabled, you benefit from the temporary suppression of all rat clutter except for the active net you are routing.



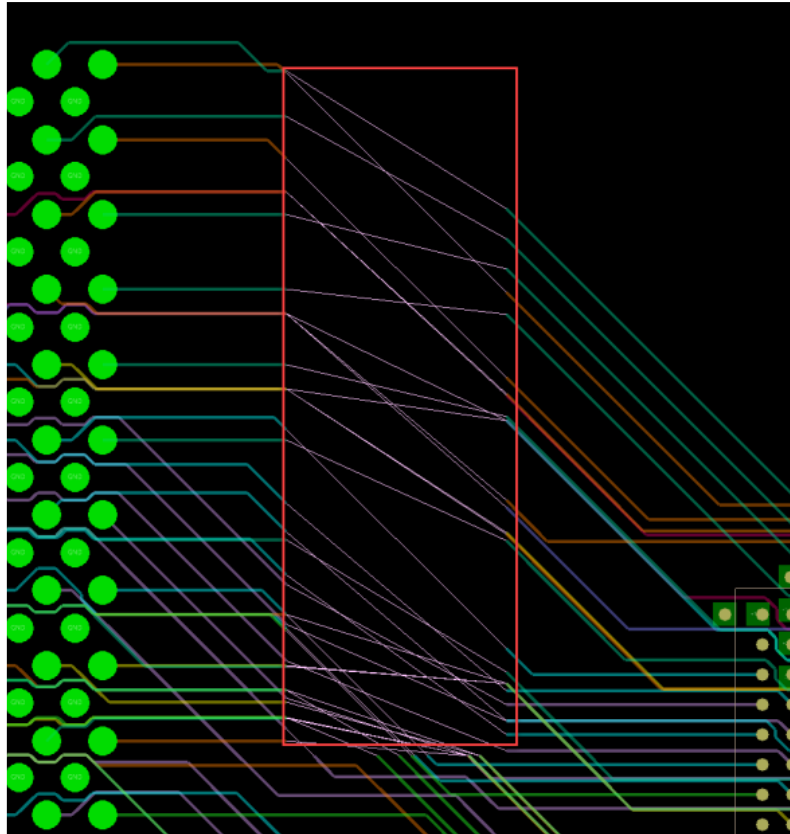
Cutting Clines (All Levels)

Two commands located in the Manufacture menu (OK not obvious) that could be leveraged to make cuts in your route path.

1. Manufacture – Drafting – Delete by Rectangle

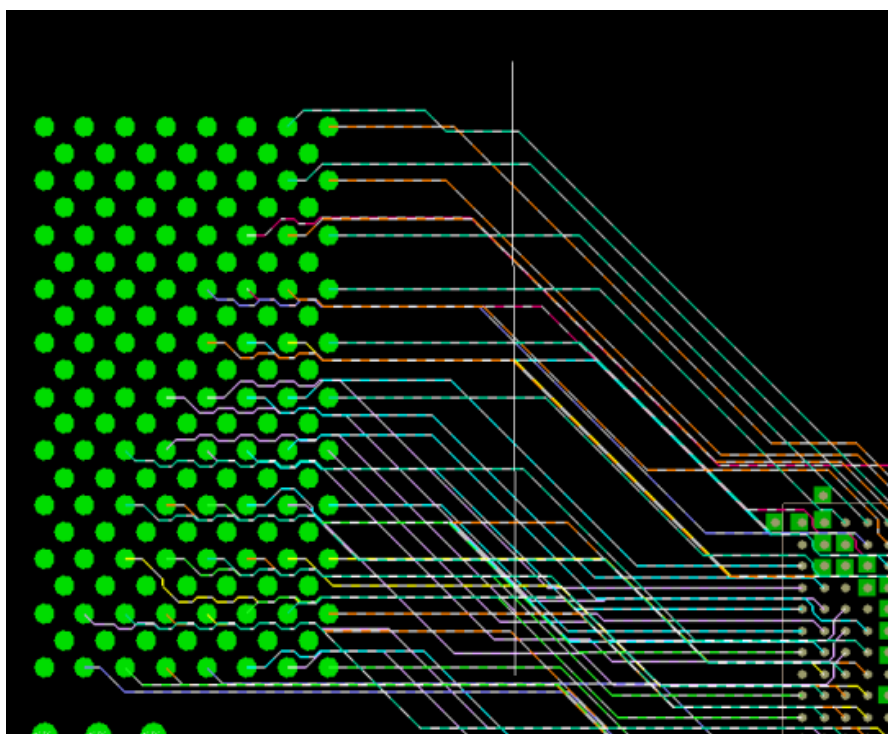
- Select the routes you wish to cut
- Draw the cut rectangle

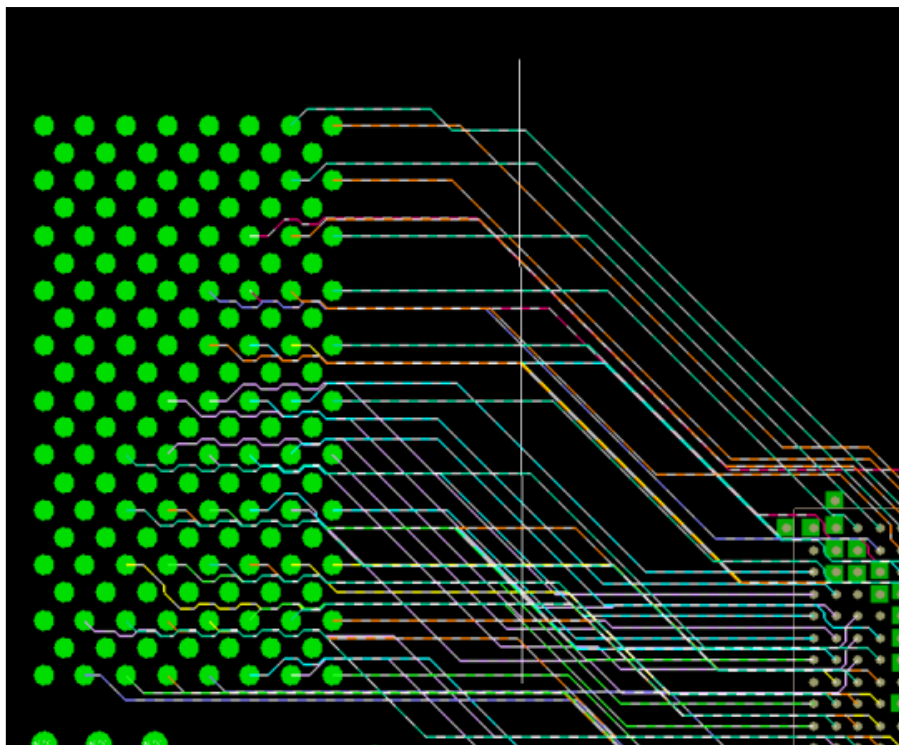
Hint – follow instructions in the command window if you experience difficulty.



2. Manufacture – Drafting – Delete by Line

- Select the routes you wish to cut
- Draw a line across the routes
- Select side of line to make the cut





Checking for max stacked via depth (Allegro Venture or Enterprise)

This check requires the “Venture” or “Enterprise” product where advanced DfX checks are available. Navigate to the Manufacturing domain then Design for Fabrication section. Select the category “holes” then apply the max stacked via count value to the CSet. As with other CM domains, apply this section to the Design section.

Allegro Constraint Manager (connected to Allegro Venture PCB Designer Suite 17.4) [DEMOP-placed] - [Manufacturing / Design for Fabrication / DFF Constraint Set]

File Edit Objects Column View Analyze Audit Tools Window Help

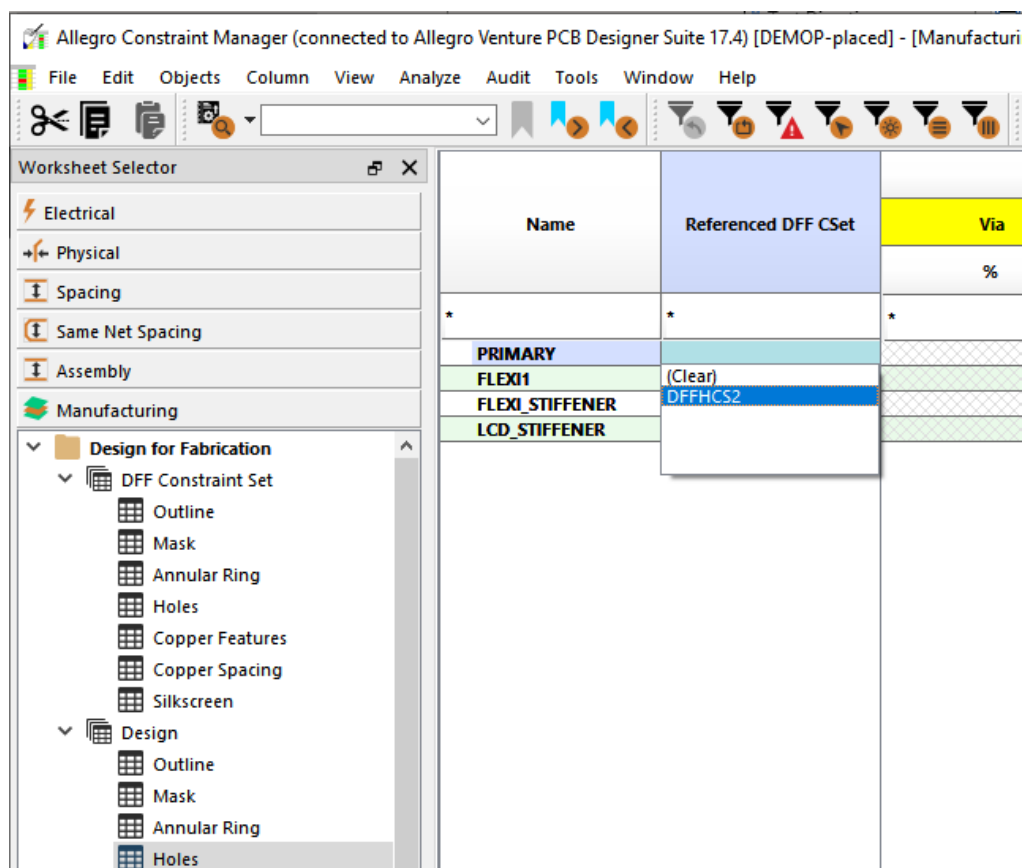
Worksheet Selector

- Electrical
- Physical
- Spacing
- Same Net Spacing
- Assembly
- Manufacturing
 - Design for Fabrication
 - DFF Constraint Set
 - Outline
 - Mask
 - Annular Ring
 - Holes
 - Copper Features

Table:

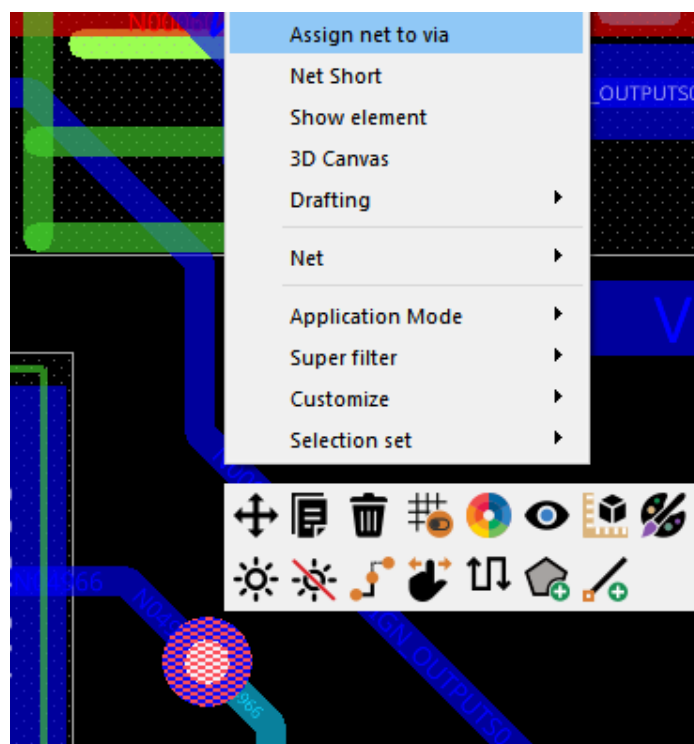
Name	Constraint set usage	kip via	Max stacked via count	Maximum stacked uvia count	Maximum count of uvias stacked on core via
*	*		*	*	*
<Create new>					
DFFHCS2	Stackup		4		

The image below shows the applying of the CSet



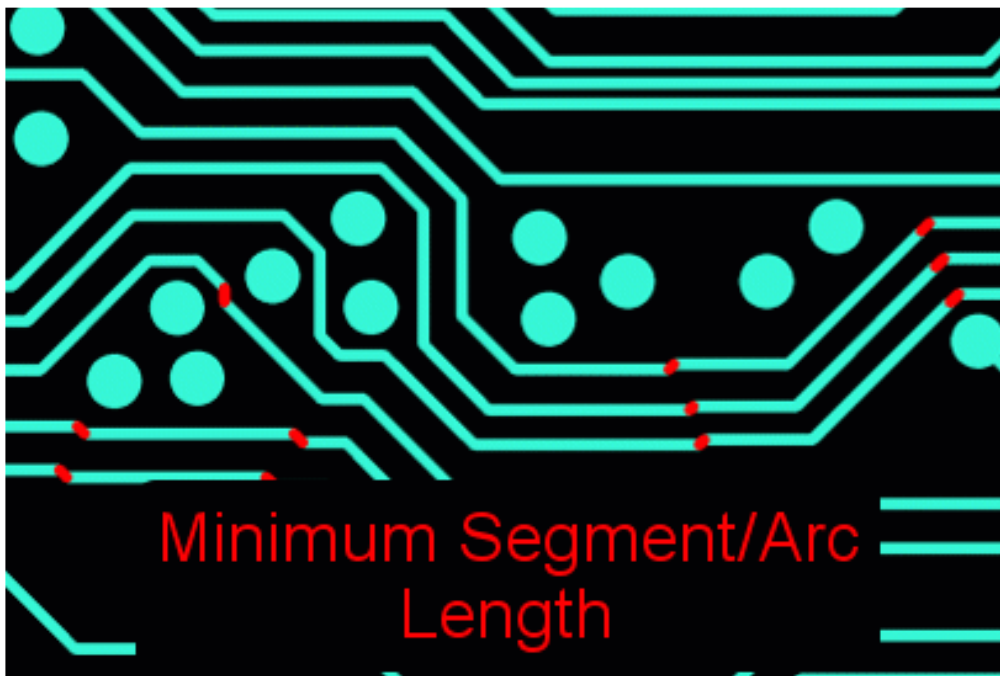
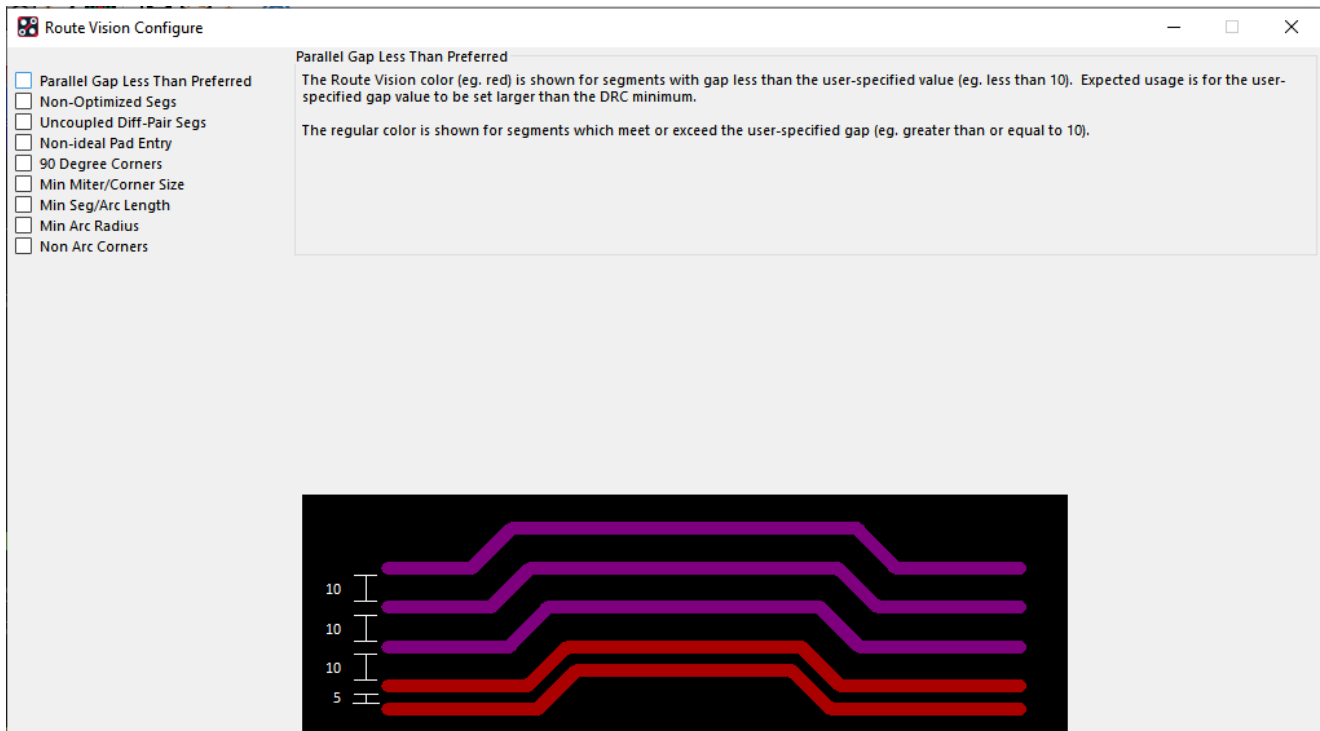
Assign net to vias (All Levels)

Offered previously as a skill app, general and etch edit modes now offer this command using the right click context sensitive menu. Hover over a via(s) then right click – Assign net to via. Refer to options pane for netlist pulldown or select net based element in the workspace.



Route Cleanup (OrCAD Professional and above)

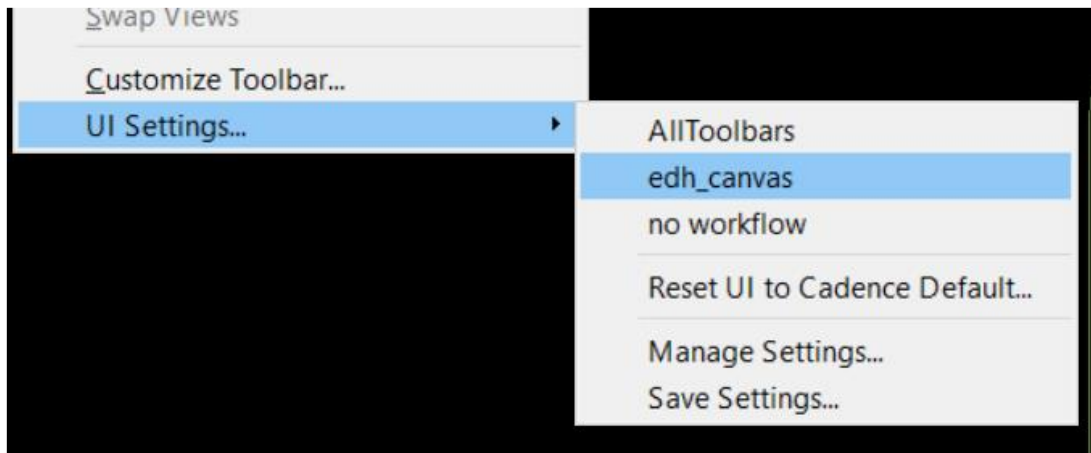
From non-ideal pad entry, short segments, 90 degree corners or non-arc corners, consider the Route Vision Application. First enable the Vision Manager (View – Vision Manager or Display – Vision Manager) then in the Options Pane, select the “Visions” tab; pick Route Vision from the pulldown. Configure your settings then click OK to invoke the command.



Save and Restore your Canvas settings All Levels)

PCB Editor offers the flexible to customize the location of the option panes and toolbar icons. If for some reason your environment is reset to the Cadence default environment, you may want to consider these steps to restore your custom environment. First step would be to establish your preferred environment.

- Save Steps: View – UI Settings – Save Settings then provide name when prompted
- Restore Steps: View – UI Settings then select name from list



Reducing Mouse Clicks & Travel (Various)

Tips to help reduce the number of mouse clicks & travel to the options panel.

Adding Vias – Use of Space Bar (All Levels)

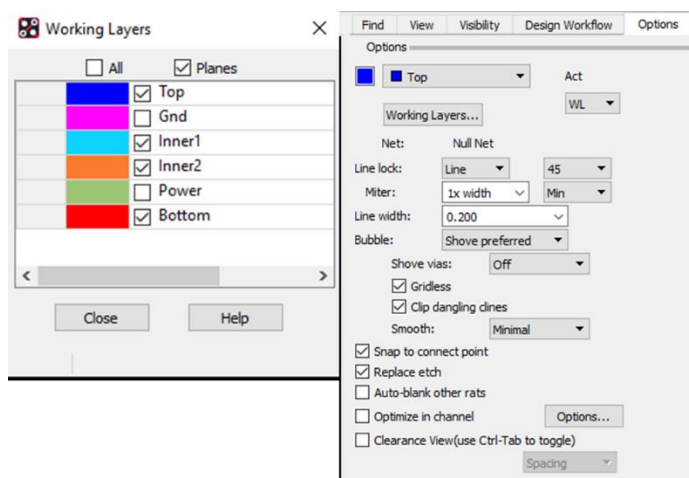
Adding a via has traditionally been done with a double left click of the mouse. The use of the space bar can save you 1000's of mouse clicks per year. I suggest adding the function key below to your local env file. The spacebar entry is represented by " ". Other keys can be assigned but space bar is easy to click without looking down.

funckey " " "pop bddrill -cursor"

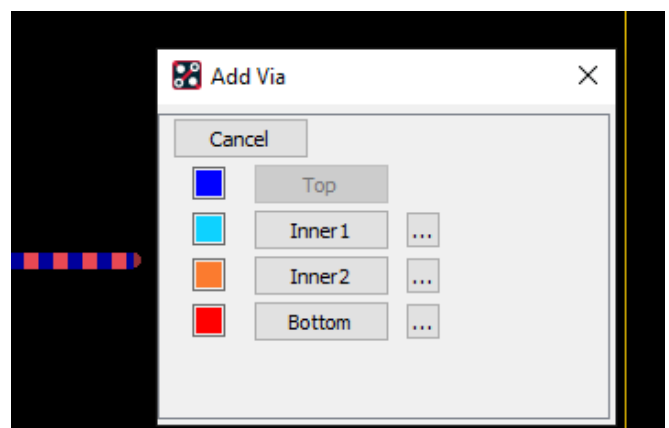
Adding Vias – “Working Layer” model (All Levels)

The Working Layer “WL” model to add vias is available in all versions of PCB Editor. It can be used to add conventional through-hole or staggered/stacked HDI vias. Select your target routing layer from a popup GUI that appears adjacent to the via insertion area.

- Order the vias in each Physical CSet
- Click on the “...” to access alternative (least preferred) vias



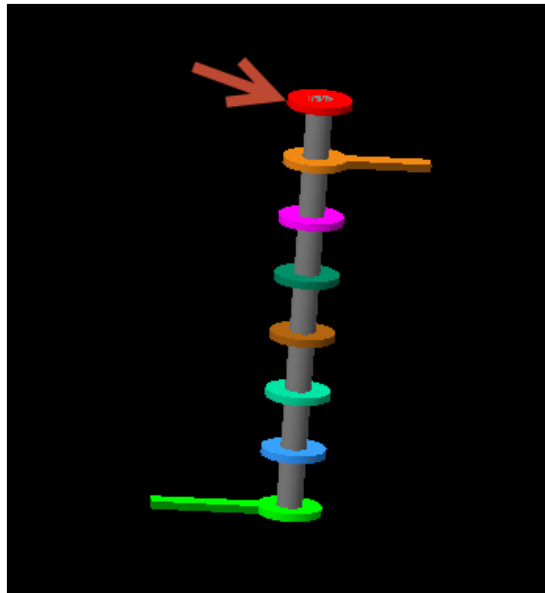
In Add Connect – Select ‘WL’



Select Target Layer during routing

Deleting a via in a stack (All Levels)

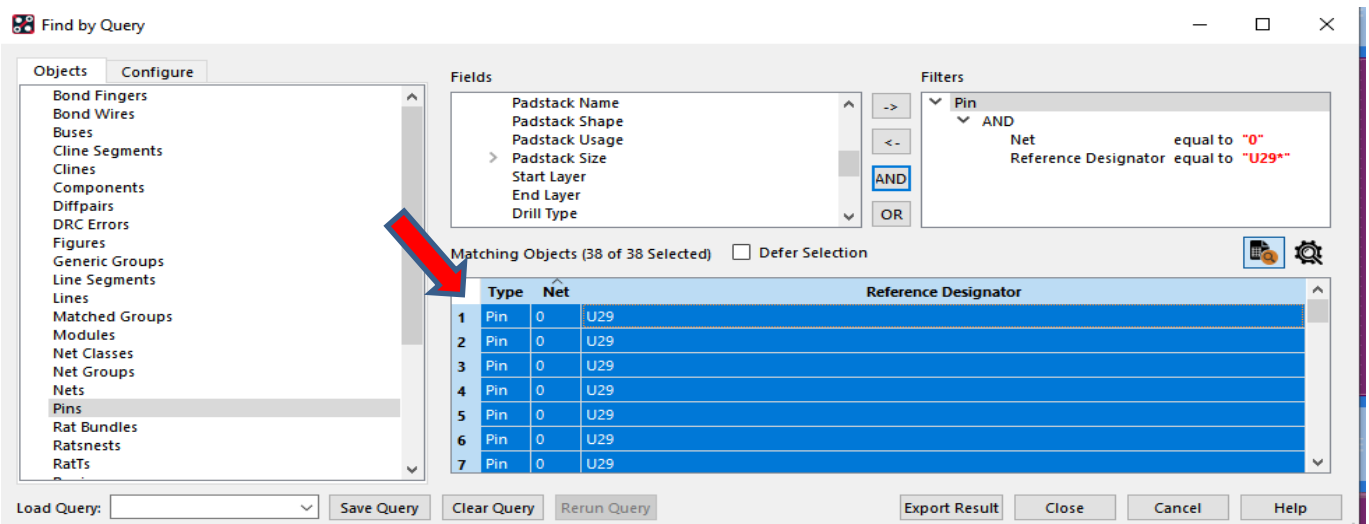
1. Use Edit - Delete, select the stacked via, and then use the right click - Split Stack command. From the popup list, select the layer pair to delete.



Highlight all GND pins on a particular component (All Levels)

Consider using the “Find by Query” function to locate elements based on qualifiers.

1. Invoke “Show Element”.
2. Open the Find Filter and select “Find by Query”.
3. Double click Pin to move it to the Fields section then double click Net and Reference Designator.
4. In this example double click Net in The Filters and change it from equal to * to equal to 0.
5. Repeat this process for Reference Designator but set it to U29*.
6. Candidate objects are listed and can be selected by left clicking the required pin number or select the white box between rows and columns to select all. This will select all objects in the main canvas so you can use the Find by Query without an active command then right click on the object(s) and choose the required action.



Add Connect – Single click execution (All Levels)

In Etch Edit Application Mode, make a single pick on a pin, via or rat to begin Add Connect. Ensure “Enable Single Pick Execution” mode is enabled. Access this option from the right click – Customize menu.

Add Connect – Add a vertex using a Funckey key (All Levels)

Instead of using a left click to add a vertex point during Add Connect, consider using a Function Key. Simply click the X key every time you want to add a vertex during routing.

```
funckey x "pick_to_grid -cursor"
```

Slide – Single Click Execution (All Levels)

In Etch Edit Application Mode, make a single pick on a cline segment to slide it.

Change Active/Alternate Layers using Function Keys (All Levels)

Increment or decrement the active or alternate layer

```
funckey + subclass ++ (use of “+” character to increment active subclass)
```

```
funckey - subclass -- (use of “-” character to decrement active subclass)
```

```
funckey a altsubclass ++ (use of “a” character to increment alternate subclass)
```

Directly change the active layer

```
funckey 1 options subclass TOP
```

```
funckey 2 options subclass SIGNAL_2
```

```
funckey 3 options subclass SIGNAL_3
```

```
funckey 4 options subclass SIGNAL_4
```

```
funckey 5 options subclass SIGNAL_5
```

```
funckey 6 options subclass SIGNAL_6
```

```
funckey 7 options subclass SIGNAL_7
```

```
funckey 8 options subclass BOTTOM
```

Another method to change the active subclass is from a right click:

Right click > Change Active Layer

Deleting Elements using a Function Key (All Levels)

I think I use this function key more than any other one. Just pass your cursor over a cline, segment, via, text or shape and click “d” to delete it. No click of the mouse!

```
funckey d "prepopup; pop dyn_option_select @:@Delete"
```

Moving Components – Single click execution (All Levels)

In Placement Application Mode, make a single left click pick on a component to move it.

Rotating a Component using a Function key (All Levels)

Click the function key R to rotate a component during movement

```
funckey r iangle 90
```

Mirror a Component using a Funkey Key (All Levels)

Click the function key M to mirror a component during movement

```
funkey m "pop mirror"
```

Snapping using a Funkey Key (All Levels)

While moving an object, use a function key to snap to various elements.

```
funkey f "prepopup;pop dyn_option_select 'Snap pick to@:@Figure'"
```

```
funkey i "prepopup;pop dyn_option_select 'Snap pick to@:@Intersection'"
```

```
funkey c "prepopup;pop dyn_option_select 'Snap pick to@:@Arc/Circle Center'"
```

```
funkey v "prepopup;pop dyn_option_select 'Snap pick to@:@Via'"
```

Alias commands to the Middle Mouse Wheel (All Levels)

The “button” command can be used to alias the Middle Mouse Wheel to commands; works with SHIFT, CONTROL and SHIFT-CONTROL combinations.

Examples:

```
button Swheel_up subclass -+
```

```
button Swheel_down altsubclass -+
```

```
button Cwheel_up "roam y -$roamInc"
```

```
button Cwheel_down "roam y $roamInc"
```

```
button SCwheel_up "roam x -$roamInc"
```

```
button SCwheel_down "roam x $roamInc"
```

In Constraint Manager, those of us with ‘older eyes’ can use the CTRL + Middle Mouse Wheel to increase the font size.

Find Components or Nets quickly (All Levels)

Use CTRL+F for Components and CTRL+N for nets, then simply type the refdes or netname required. The component or net is highlighted and the item is zoomed to and centred.

```
alias ~F "prepopup ; pop dyn_option_select 'Selection set@:@Clear all selections';set prompt;prompt 'Find Ref Des';refdes $prompt;zoom selection"
```

```
alias ~N "prepopup ; pop dyn_option_select 'Selection set@:@Clear all selections';set prompt;prompt 'Find Net Name';net $prompt;zoom selection"
```

Replacing Padstacks by window selection (All Levels)

In General Edit Application Mode, window around the set of pins or vias you wish to change then use the right click > Replace Padstack > Selected Instances command.

Optional selection window (All Levels)

If a polygon selection window is desired;

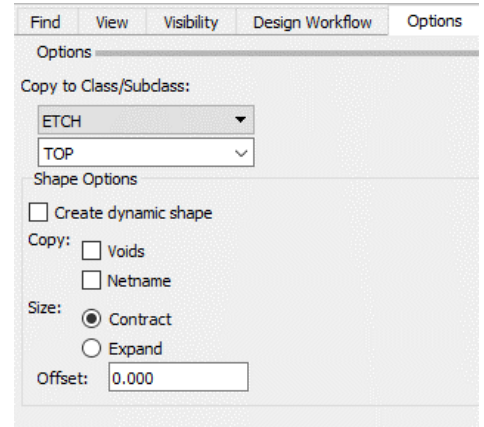
Right click > Selection Set > Select by Polygon, Lasso, On Path.

Z-Copy – a powerful utility (All Levels)

This is a basic function that everyone should know.

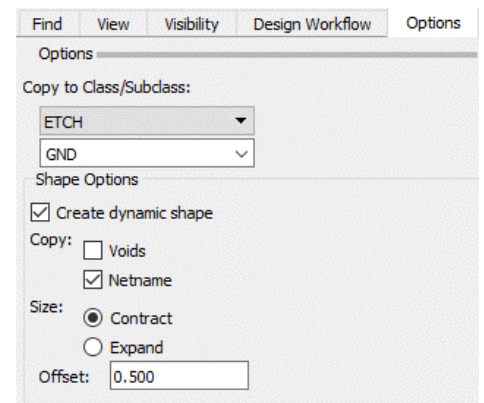
Create a Route Keepin area derived from the board outline

Select Edit Z-Copy(Allegro) or Shape Z-Copy (OrCAD), adjust the options settings to class = ROUTE KEEPIN, Subclass = ALL. Enable 'contract' then enter value the route keepin will be offset from the board outline. Last step is to select the board outline.



Did you know Z-Copy can be used to copy to multiple layers at once?

For example, you wish to create multiple GND planes but the names of each subclass end in GND_5, GND_8, GND_13, etc. Use Z-Copy then in the options tab select one of the GND layers. Edit the numerical part of the layer then enter the wildcard '*' as shown in the graphic below.



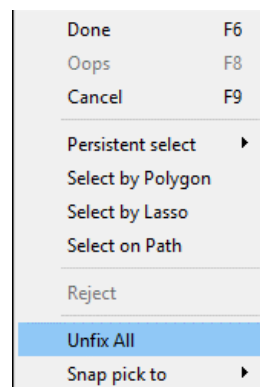
Fix/Unfix Elements in the Design (All Levels)

Tips to add and remove the Fixed Property

Quickly unfix all elements

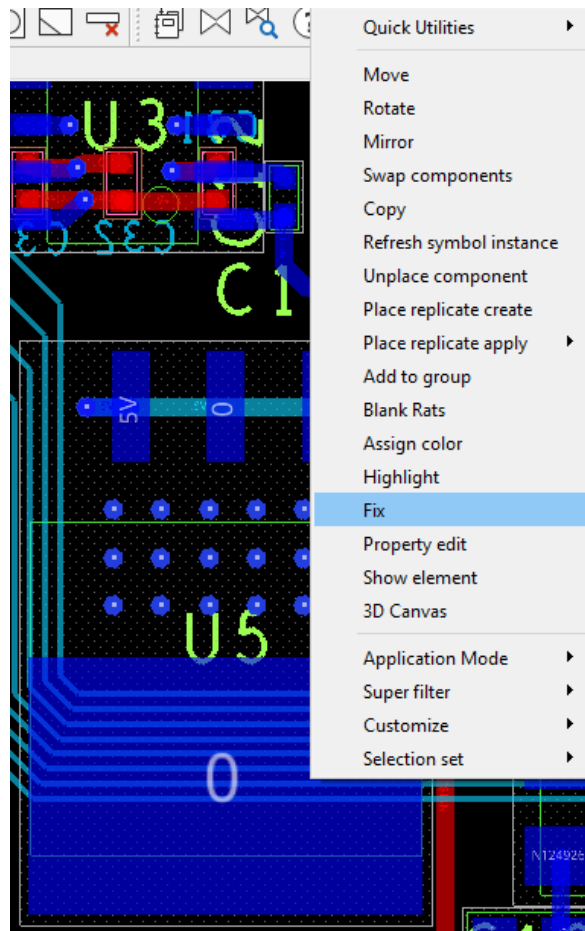
The quickest method to remove the fixed property from all elements in the Design is to:

1. Click the Unfix Icon
2. Then right click > Unfix All



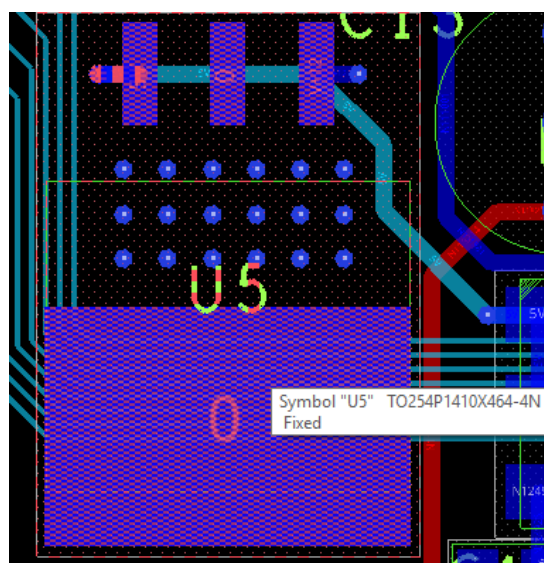
Fix a Symbol's location

Simply hover over the symbol then select the “Fix” command from the context sensitive right click menu.

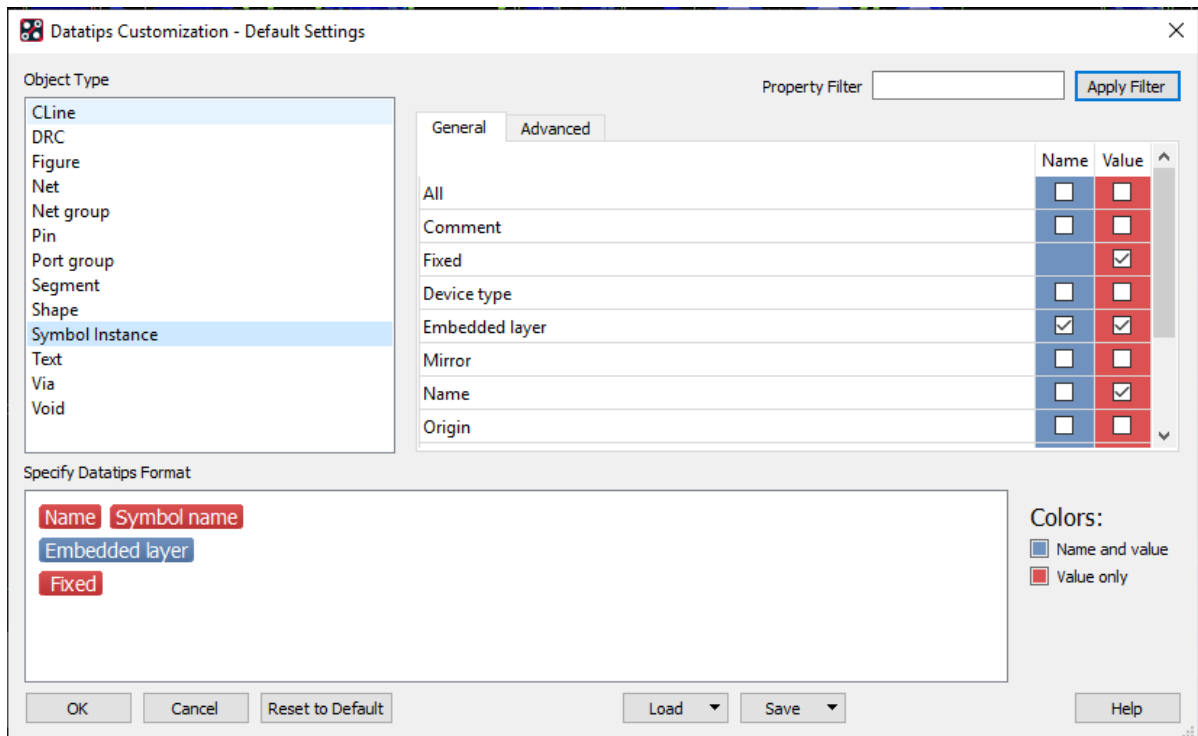


Datatip display of the Fixed property

You would like to know whether an element is fixed while hovering over it.



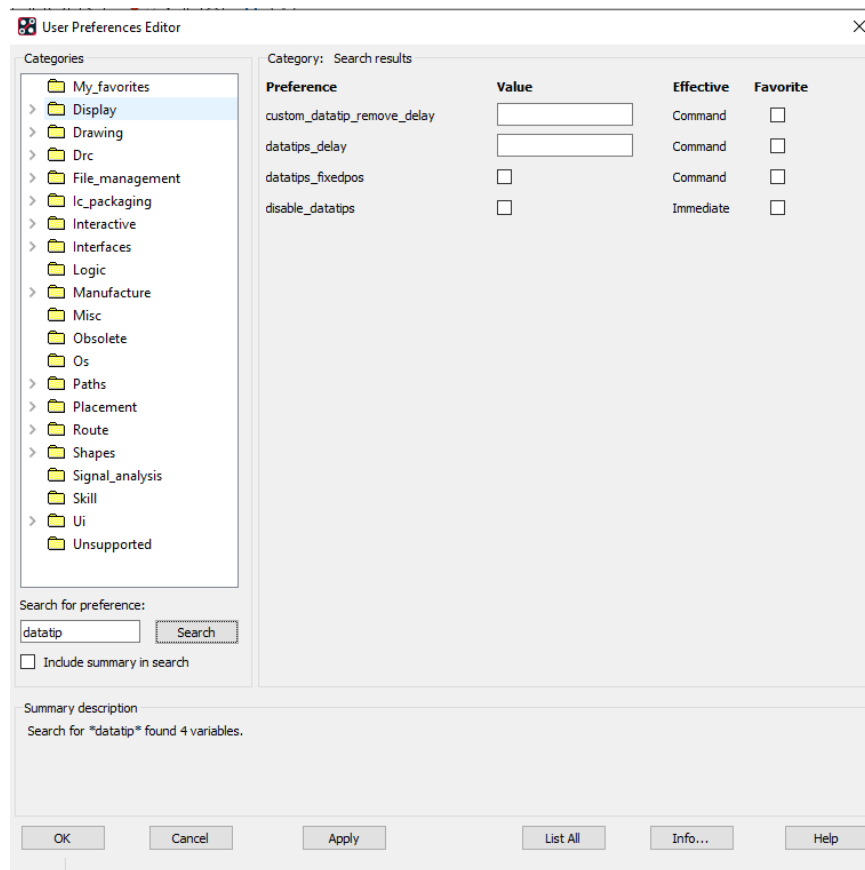
Configure the datatip setting as shown below. You may want to enable other symbol related properties to also display in the datatip window. This is done from the Setup > Datatip Customization menu. Select symbol Instance under Object Type then enable the value for “FIXED”.



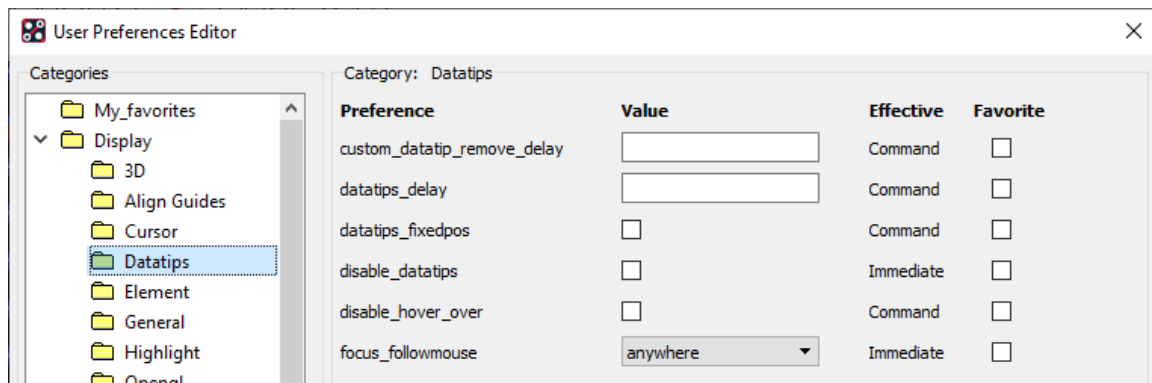
Datatip Options (All Levels)

Controls for delay, location and disablement

The User Preference Editor contains hundreds of variables. The “Search” box is a very handy mechanism. In this example, I type in the word “datatip” then click Search. Variables to delay, locate and disable datatips are available to you.

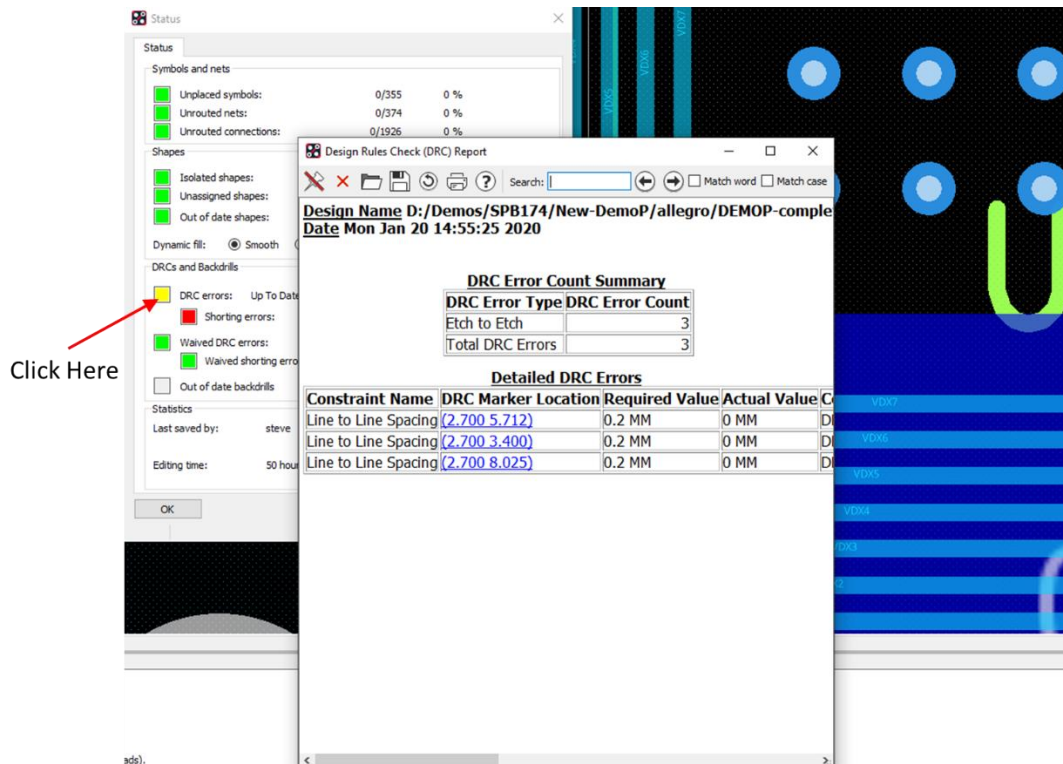


The complete set of variables related to Datatips is located in the Display > Datatips Category



Status Form traffic lights (All Levels)

Display > Status (Allegro) or Check > Design Status (OrCAD) Did you know you can click on the swatch to obtain a report?



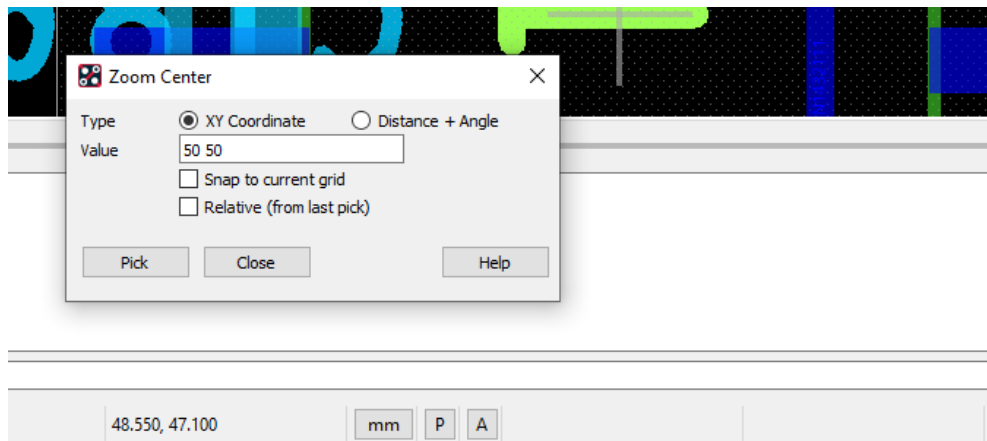
“Go to” X,Y Location (All Levels)

Navigate to an X,Y location in the Design

You wish to quickly go to a specific X, Y location in the Design; e.g.: go to location x = 50, y = 50.

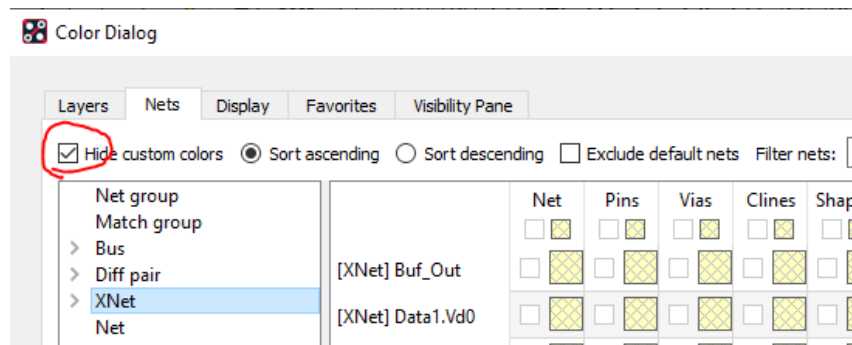
Adjust your zoom level then make a click on the ‘P’ button located at the base of the canvas display. Enter in your coordinates then click ‘Pick’

Note – Ensure you set application mode = none for this behaviour



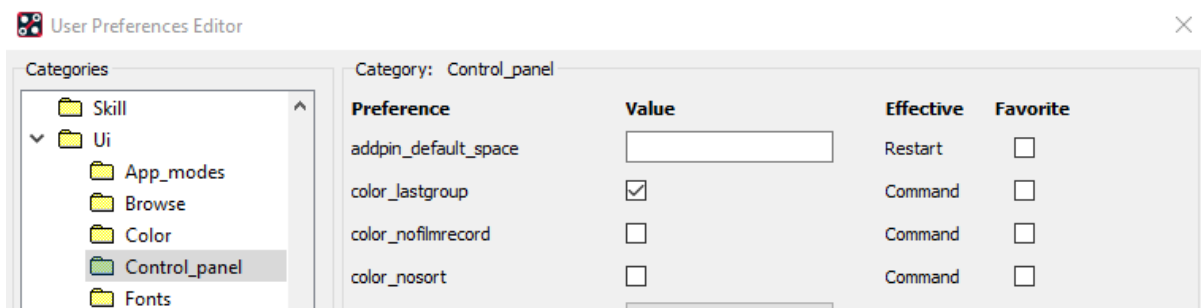
Disabling Custom Color Assignments (All Levels)

You may inherit a board from another designer or shop and question some of the colour assignments. One quick method to disable colour overrides that may have been applied to nets, buses, Diff Pairs is to go into the colour form. Select the 'Nets' tab on top, you will see a button called 'Hide Custom Colors'. Select that option to revert to 'layer' based colouring.



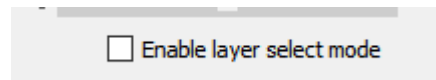
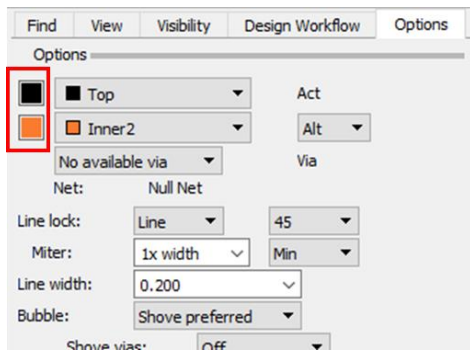
Color Dialog – Open last folder used (All Levels)

Set the variable color_lastgroup located in Setup - User Preferences - UI - Control_panel



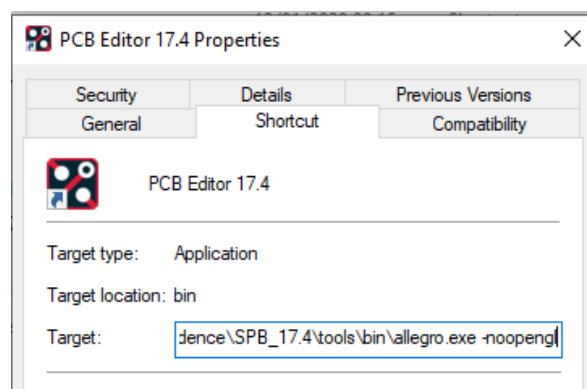
Display a Layer (All Levels)

Click the color swatch box to the left of the subclass in the Options pane to quickly turn layers on/off during a command. You can also use the Enable Layer select mode in the Visibility tab to quickly turn layers on / off.



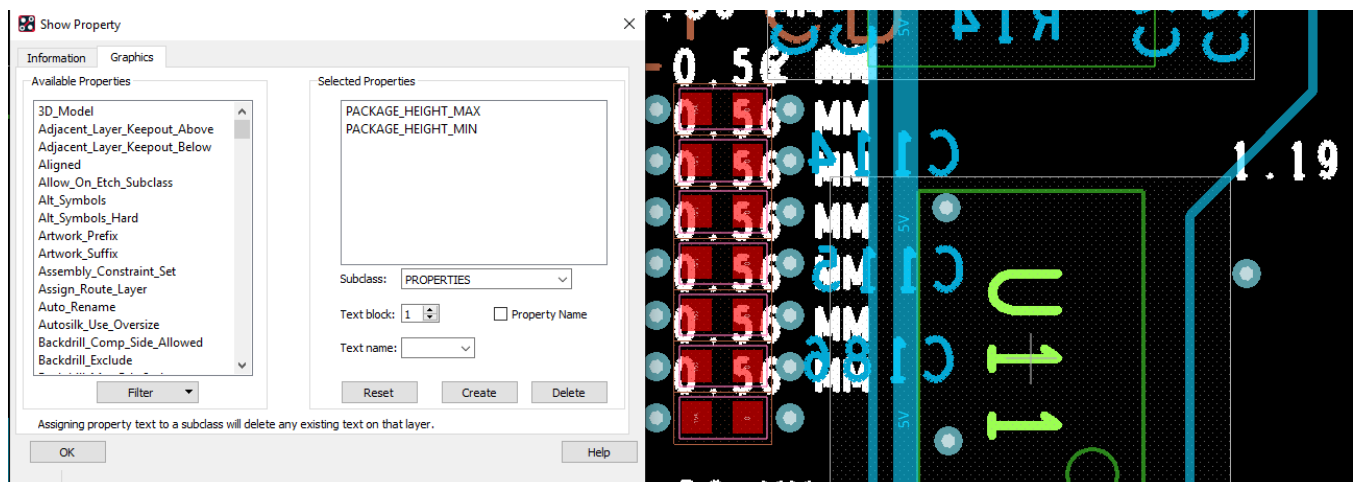
Invoking Allegro in No OpenGL mode (All Levels)

It may be necessary to run Allegro in a No OpenGL mode; for example, hosting a Net Meeting. Consider creating a Desktop Shortcut for Allegro.exe with the `-noopengl` option.



Display of Properties in the Canvas (All Levels)

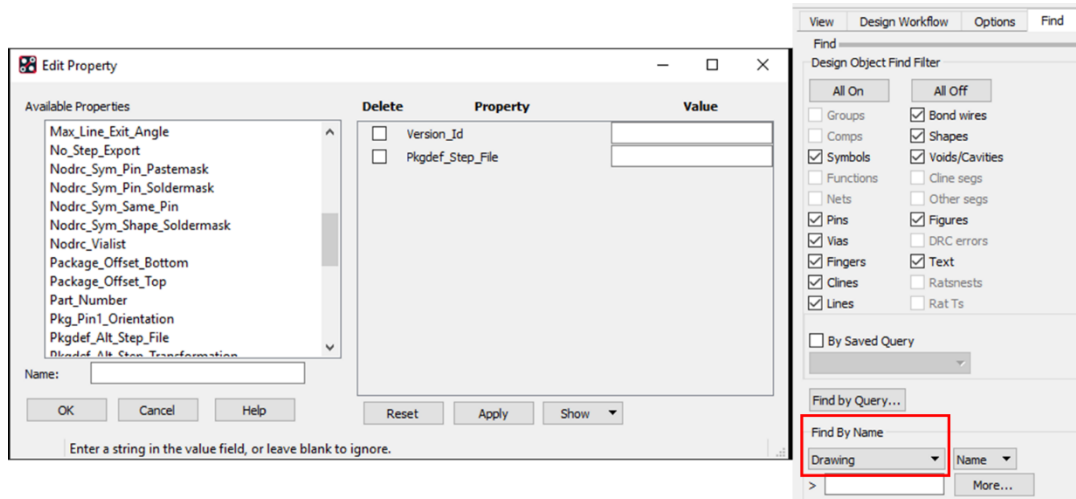
Any property attached to an element can be displayed in the canvas. From the Display > Property (Allegro) or Check > Properties (OrCAD) menu, select the Graphics tab then select properties to display from the left column. Clicking the Create button writes out the property values and/or their name to the Class > Manufacturing, Subclass > Properties.



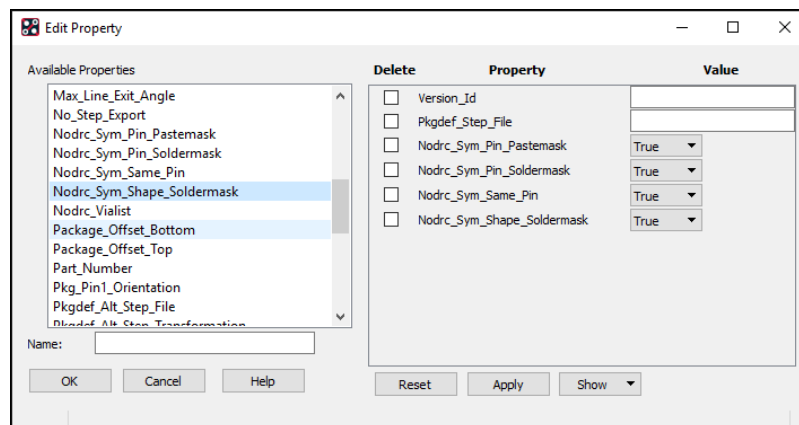
Suppress Pin-Pin Violations within the same symbol (All Levels)

PCB Designers often use Constraint Regions to suppress pin to pin violations within the same symbol. The property 'nodrc_same_sym_pin' can be applied to the symbol but did you know it can also be applied to the drawing? Applying it at the drawing level has a global impact to all symbols.

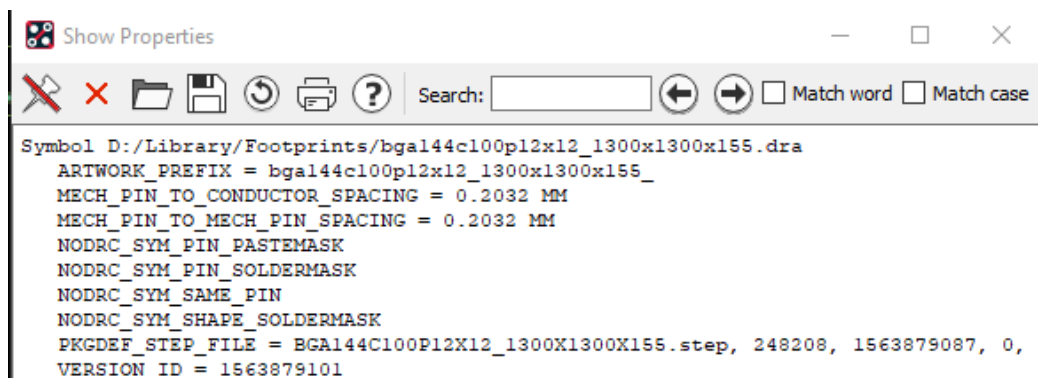
1. Open the filename.dra
2. Edit > Properties > then select Drawing in the Find by Name field.



3. Choose the required Properties on the left, they are added to the right. There are other Nodrc_Sym properties to include if required.



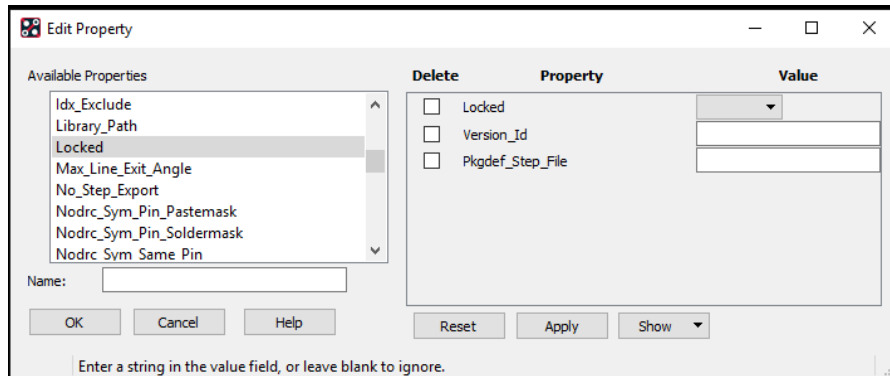
4. Click Apply and the properties are added to the Drawing.



Locked property (All Levels)

The Locked property was designed for Re-Use modules but did you know

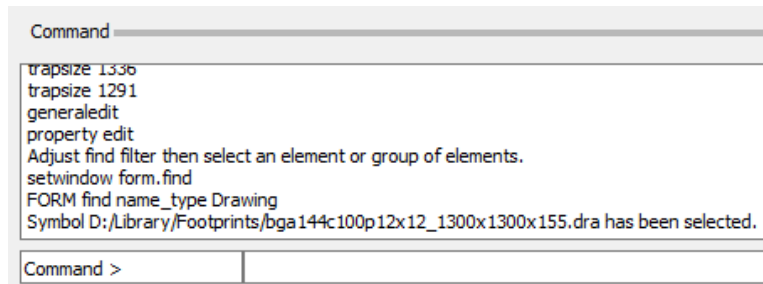
The property can be applied to a place replicate circuit to prevent accidental movement of its members. It can also be applied to a package symbol to prevent editing/deletion of the assembly outline or other data elements. Suggestion – consider applying the locked property to the symbol drawing file (at the library level).



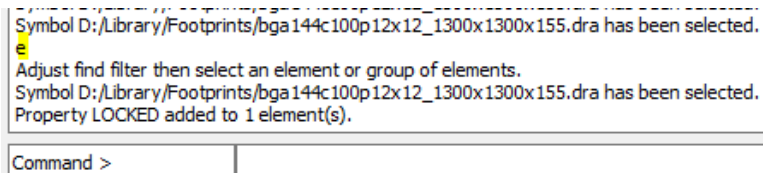
Creating a Command Shortcut with Scriptmode +e (All Levels)

Adding a drawing level property in the previous tip was labour intensive. Let's create a shortcut.

1. Enter scriptmode +e in the command window. This echoes the commands you enter.



2. Copy all the commands above to a single line
3. Separate with semi-colons
4. Map to a function key
5. funckey e "property edit;setwindow form.find;FORM find name_type Drawing;FORM find find_by_name;FORM findname objlist 'Drawing Select';FORM findname done"
6. Click the "e" key then press "ENTER" in the command window to launch the property editor dialog!!
7. Ideally set this in your env file (located in %HOME%\pcbenv) so this is available in every design.



Scriptmode +I (All Levels)

"scriptmode +i" is really a shorthand for "scriptmode +invisible"

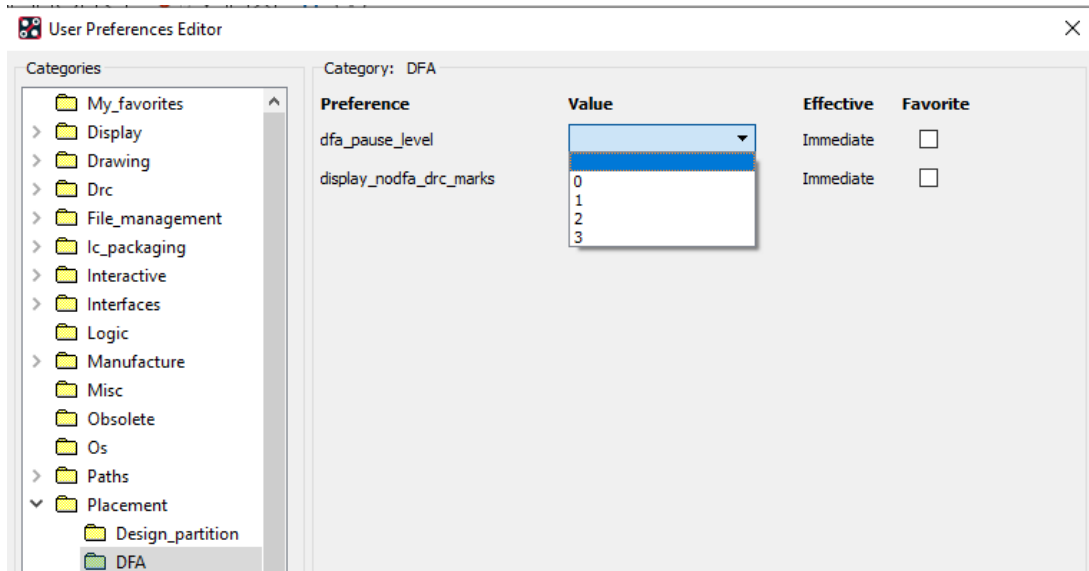
Let's say you want to create an alias for toggling end cap display but don't want to see the parameter form appear while executing the script.

alias ec "scriptmode +i; prmed; FORM prmedit display_enhance toggle; FORM prmedit done"

DFA Dynamics – Controlling spacing bubble resistance (Allegro PCB Designer)

Issue - When placing components to DFA rules, it's difficult to pull back the component when the bubble appears.

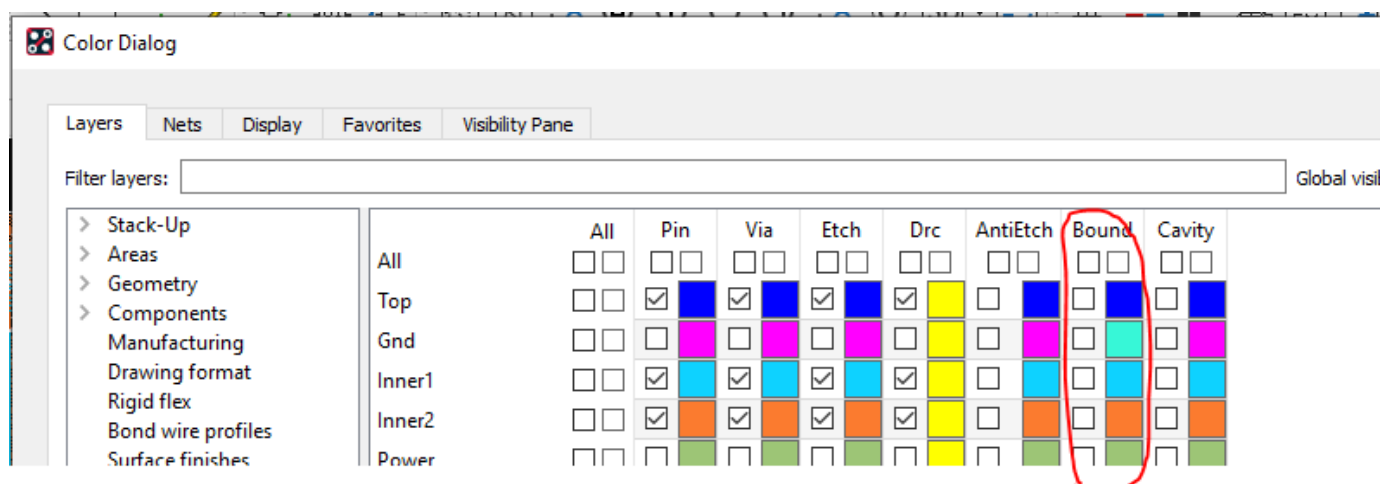
The resistance can be controlled by the "dfa_pause_level" variable located in Setup > User Preferences > Placement > DFA. Set to 0 for no resistance.



Shape has "No Etch" Status – find it (All Levels)

A dynamic shape is "out of date" BUT it is unfilled.

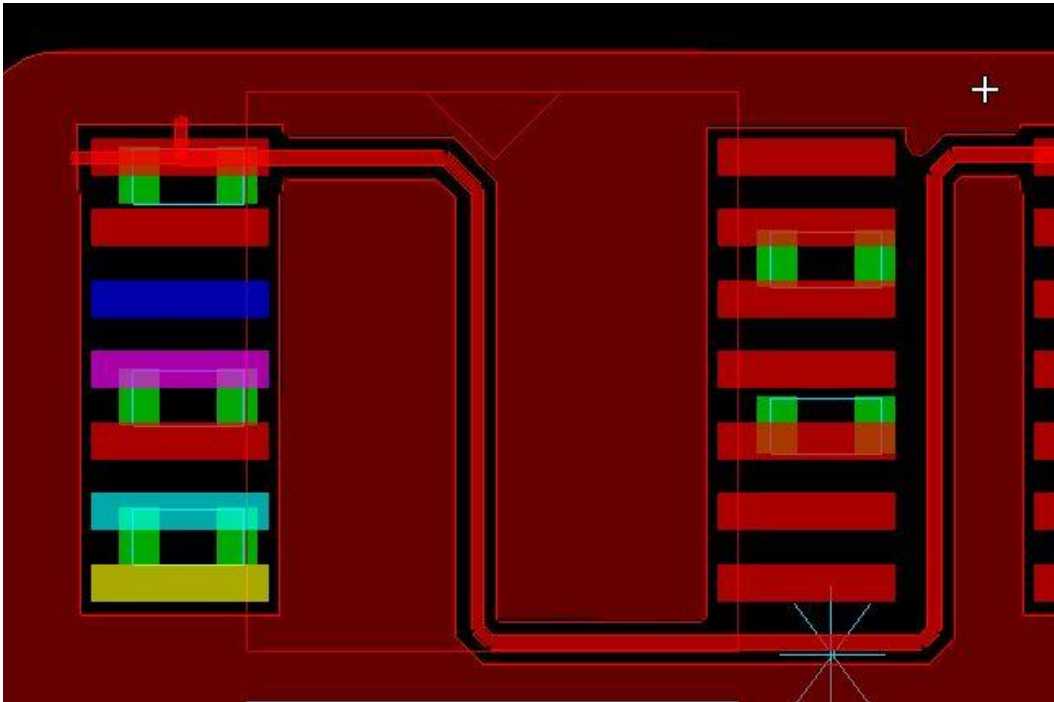
You cannot find the shape in question. It says it's at a particular XY location, on a particular layer, but there is nothing there. Turn on the 'Bound' colour item for that layer to locate the shape outline.



Voiding of GND clines through GND Plane (All Levels)

A method to auto-void GND sense lines being routed through a GND plane.

In the example below, a GND net is routed through a GND shape. The property 'void_same_net' was applied to the cline. Edit > Properties (Allegro) or Edit > Object Properties (OrCAD) then select the shape and pick the property.

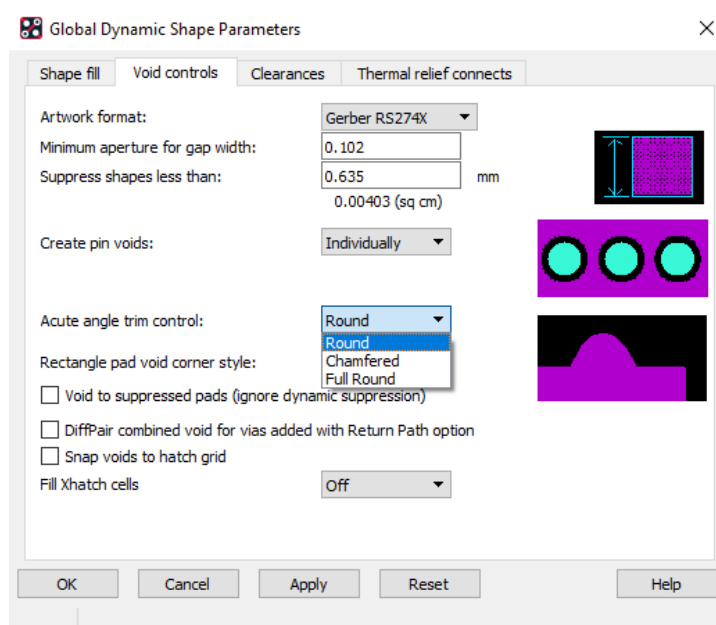


How to convert non

acute angles for shapes to round corners? (All Levels)

Use Shape > Global Dynamic Parameters > Void Controls tab and set the Acute angle control to "Full Round". Static shapes get the same capability by setting the following variable in your env file (%HOME%\pcbenv)

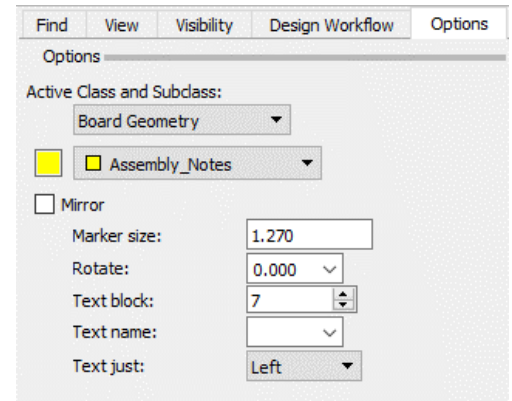
set eap_static_newsmooth env variable.



Adding Text from a file (All Levels)

Tip to add text from a .txt file on disk

- Run the add text command: Add > Text
- Set the desired text options on the Options Pane
- Position the cursor with a left click at the location that you want the first line of text to start.
- Right click and choose: Read from File

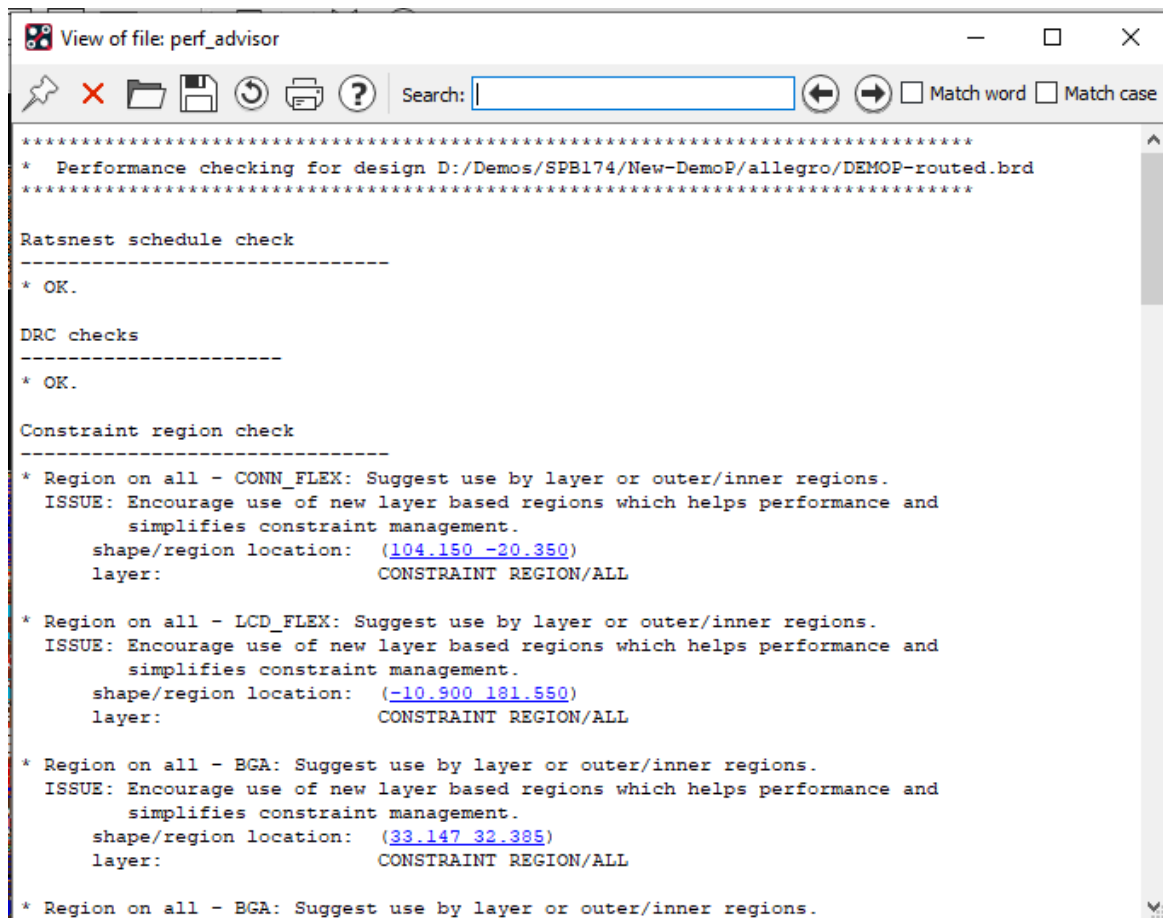


Why does the system react slowly when moving a comp? (All levels)

Most likely your large pin-count nets are scheduled Min Tree. Add a VOLTAGE property to large pin-count nets like VCC and GND by Setup > Constraints > Constraint Manager (Allegro) or Setup > Constraints (OrCAD), then on the Properties > Net > General Properties add the required Voltages to the Voltage column.

Is my Database Optimized for Performance? (All Levels)

The performance advisor provides suggestions to increase database performance. The command can be run from Tools > Database Check > Performance Advisor (Allegro) or Check > Database Check > Performance Advisor (OrCAD).



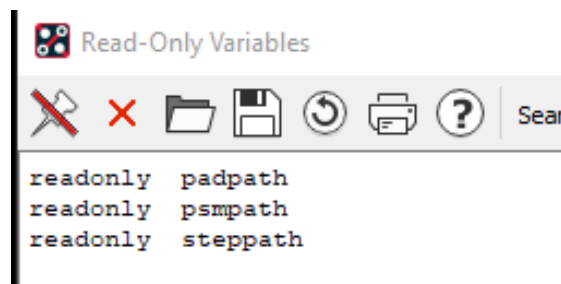
Read Only Variables (All Levels)

A method for a site administrator to make variables read only

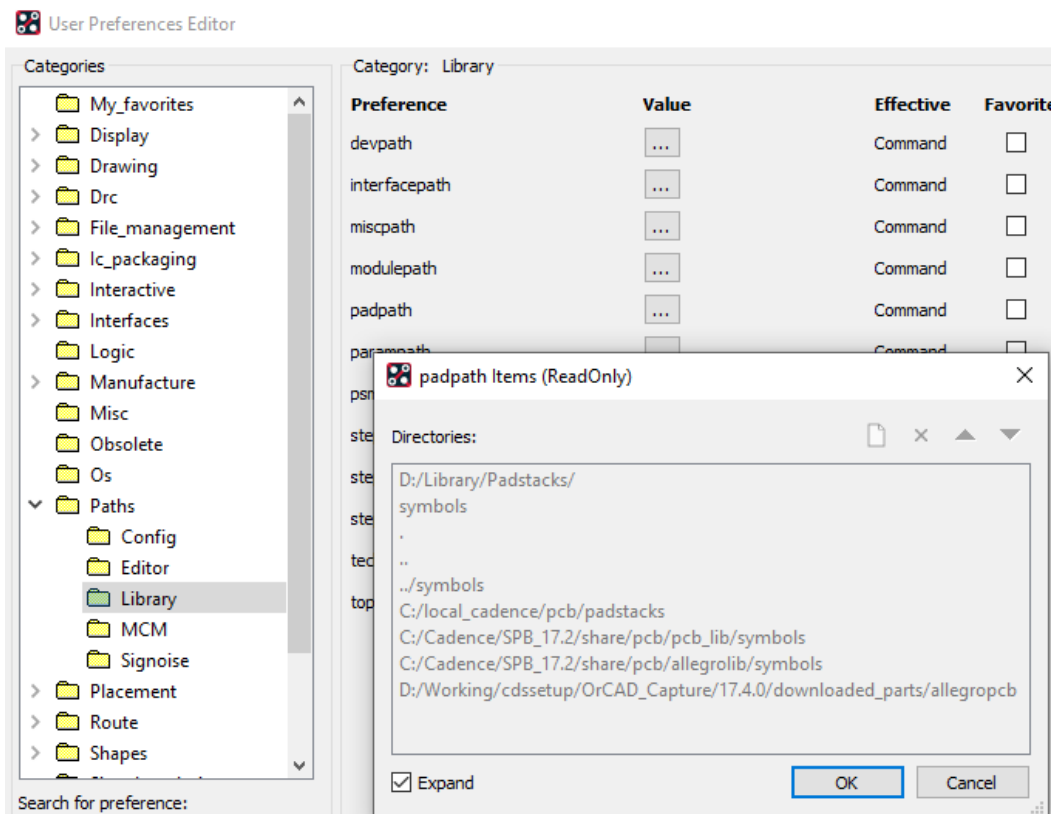
Add a readonly entry under the respective variable. In the env file (%HOME%\pcbenv) In the example below, I wish to prevent the end user from modifying PSMPATH, PADPATH and STEPPATH. The command readonly XXXpath is added just below the "set psmpath" variable.

```
set padpath = D:/Library/Padstacks/ symbols . . . ./symbols C:/local_cadence/pcb/padstack:
readonly padpath
set psmpath = D:/Library/Footprints/ . . . ./symbols C:/local_cadence/pcb/symbols C:/Cade:
readonly psmpath
set steppath = D:/Library/Step_Files/ D:/Working/cdssetup/OrCAD_Capture/17.4.0/downloaded_
readonly steppath
```

To verify in PCB Editor, type readonly at the command line prompt. The window lists variables that are readonly



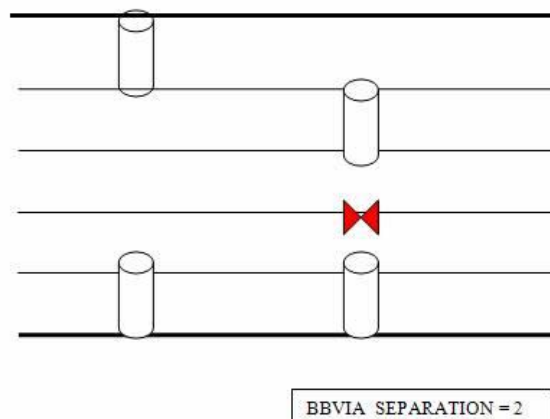
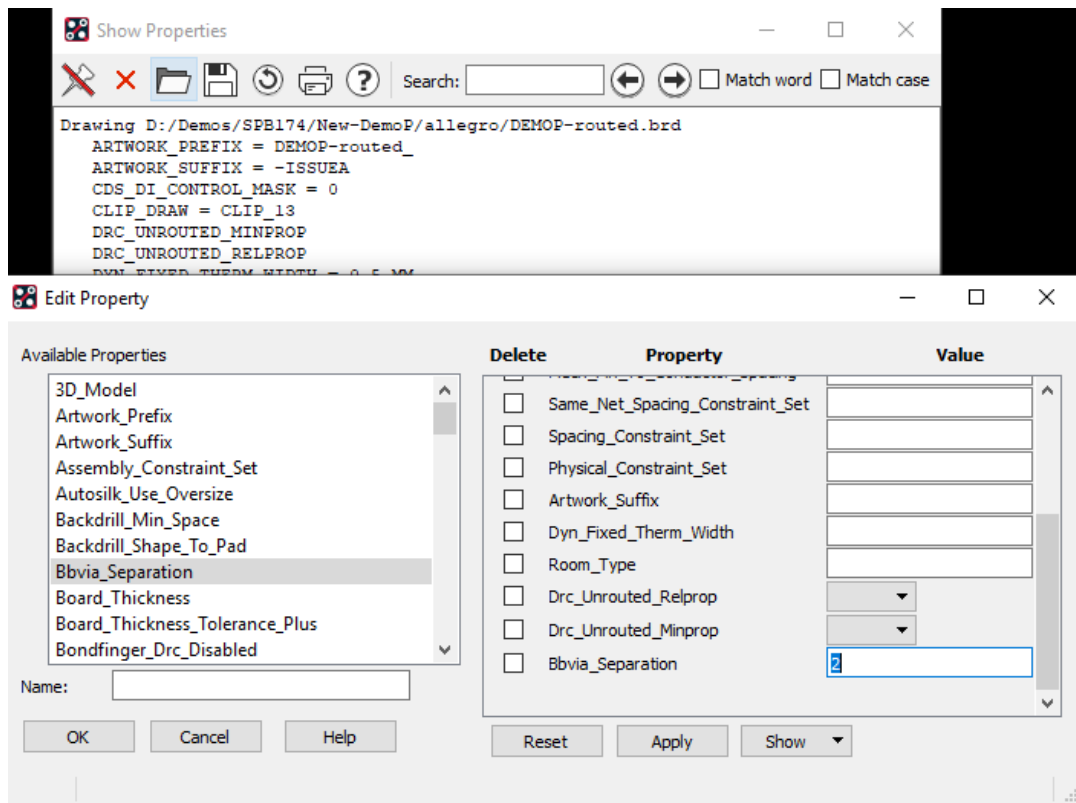
When an attempt is made to change padpath in the User Preferences editor, the values are greyed out and un-editable.:



BBVIA GAP DRC reporting too many DRCs (All Levels)

Under normal circumstances, Buried/Blind vias separated by less than the minimum bbvia gap rule will generate a DRC no matter how many layers separate them. A drawing level property, BBVIA_SEPARATION, suppresses the DRC if the vias are separated by the specified layer span value or more. In the example below, the property value of "2" suppresses the DRC on the left side. To Set this use Edit > Properties (Allegro) or Edit > Object Properties

(OrCAD) then in the Find by Name dropdown in the Find Pane select Drawing and add the BBVIA_SEPARATION property to the Drawing.

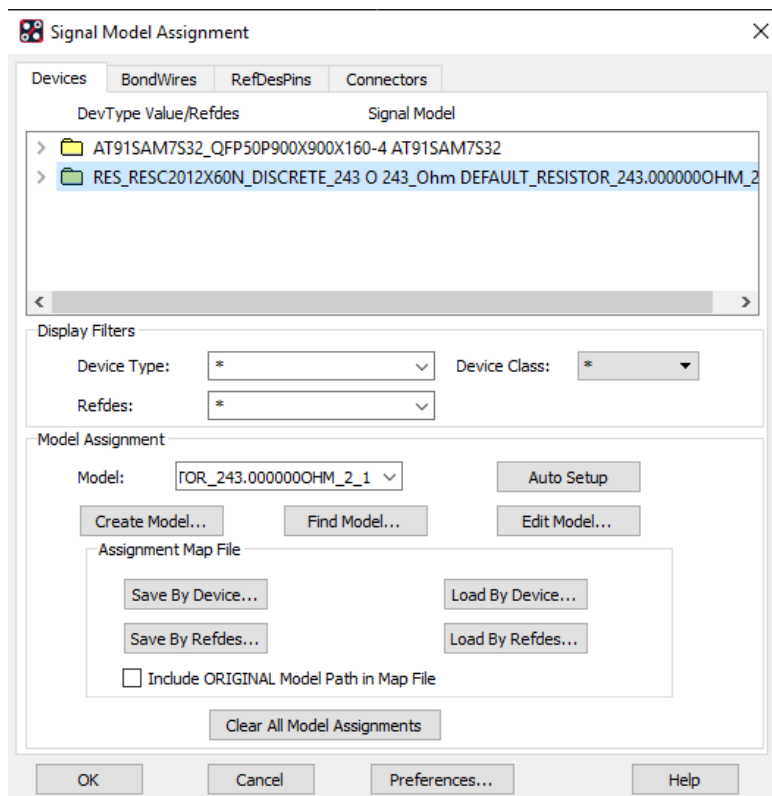


Working with Xnets (Allegro PCB Designer, OrCAD Professional)

Tips for working with Xnets

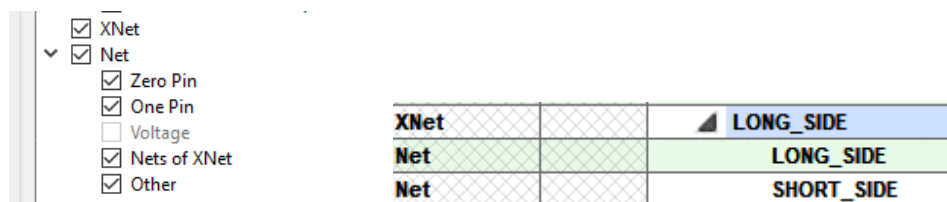
Create them – Assign default ESpice models to the discrete devices from the Analyze > Model Assignment menu. Resolve / Ignore any warnings then select the Auto Setup button to apply a default ESpice model to the discrete parts.

Note – if the schematic design is Constraint Manager enabled (CM Flow) then xnets are created automatically and the steps above are not required.



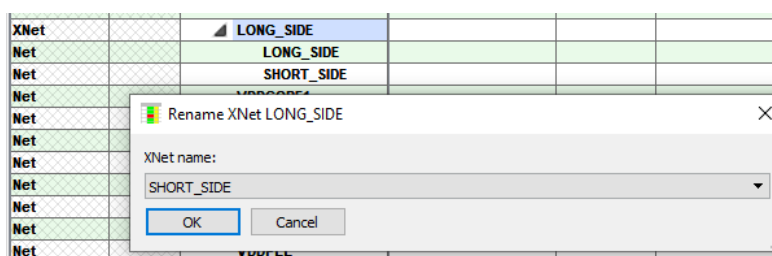
Prevent them on an Instance basis - Assign the property no_xnet_connection at the component level either directly in the board or via a property in the schematic.

Display them Xnets are now available in Constraint Manager. To view you can use Objects – Filter and turn on Nets of Xnet which will list both nets that are part of the xnet.



Naming Convention – The Xnet name defaults to the Net name with the lowest alphanumeric character. In the above example, L is before S.

Change the Xnet Name (Allegro PCB Designer only) – In Constraint Manager, select the Xnet then use RMB – Rename to choose either name of the xnet.

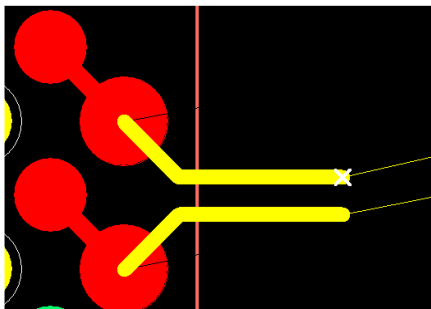
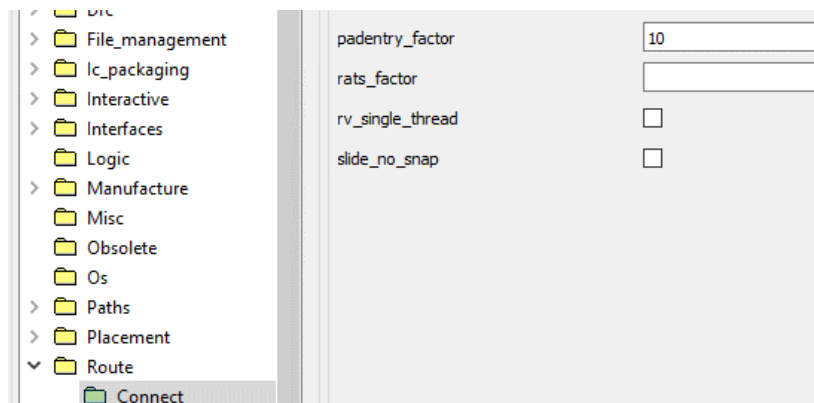


You can also control from the schematic (OrCAD Capture) which netname is used for the xnet. Add a property CDS_XNET_NAME with a value of SELECT to the net you wish to be used for the xnet name. Also ensure that you edit the allegro.cfg file (PCB – Design Sync Setup) to include CDS_XNET_NAME=Yes to the [netprops] section.

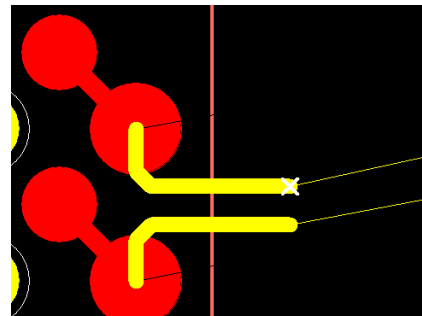
Diff Pair Gathering (All levels)

Looking for tighter coupling at the gathering location?

Decrease the value of the “padentry_factor” variable located in Route – Connect category of the User Preference Editor.



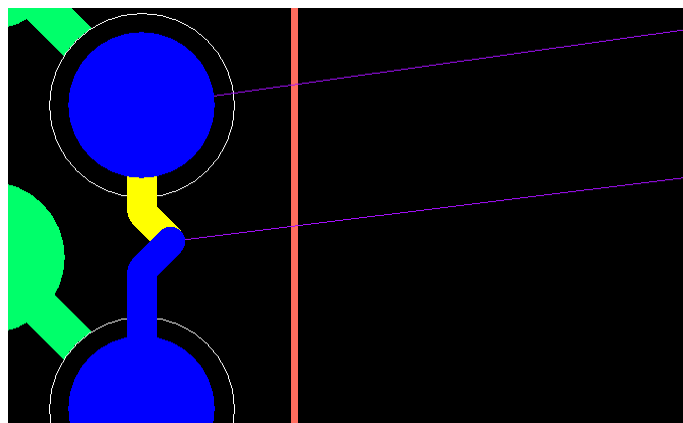
Default



Padentry set to 10

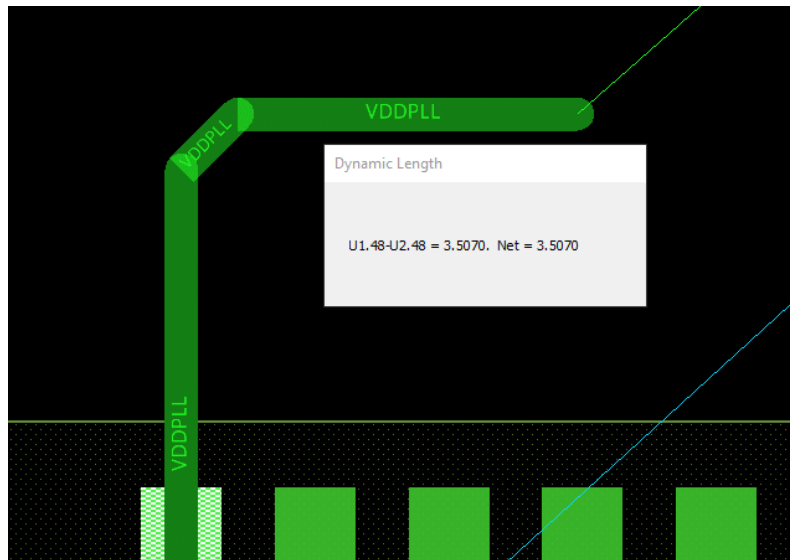
Route a Tandem Diff Pair (All Levels)

Pre route each member as shown in the graphic below then use add connect to route as a tandem pair. This assumes a Diff Pair constraint object has been created.



Display Length Meter for non constrained nets (Allegro PCB Designer, OrCAD Professional)

Set the variable “allegro_etch_length” located in user preferences > Route > Connect

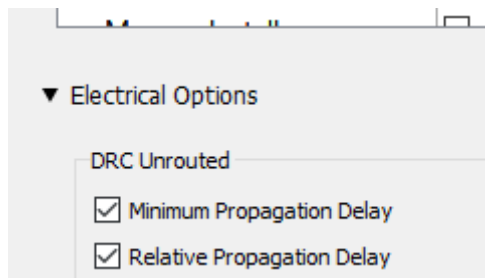


Constraint Manager (Various)

A few tips related to Constraint Manager

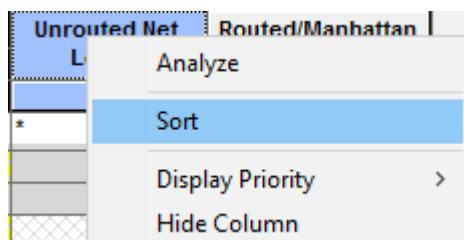
Display propagation delay for unrouted nets in CM. (Allegro PCB Designer, OrCAD Professional)

Enable the “unrouted” modes in Constraint Manager > Analyze > Analysis Modes > Electrical



Sort results from worst case to best case margin (All Levels)

Double Click Margin Column Header or right click > Sort



Display just the Failed Results (All Levels)

Use Objects – Filter Header and enable Failed only checkbox or simply click on this Icon



Display just nets that have constraints on them? (All Levels)

Use Objects – Filter Header and enable Objects with Directly Set values or simply click on this Icon



Segregate sections of CM with divider lines, i.e. identify the transition between buses and matched groups. (All Levels)

In CM, View > View Options > unsupported and Enable 'Object Type Dividers' or simply click on this Icon



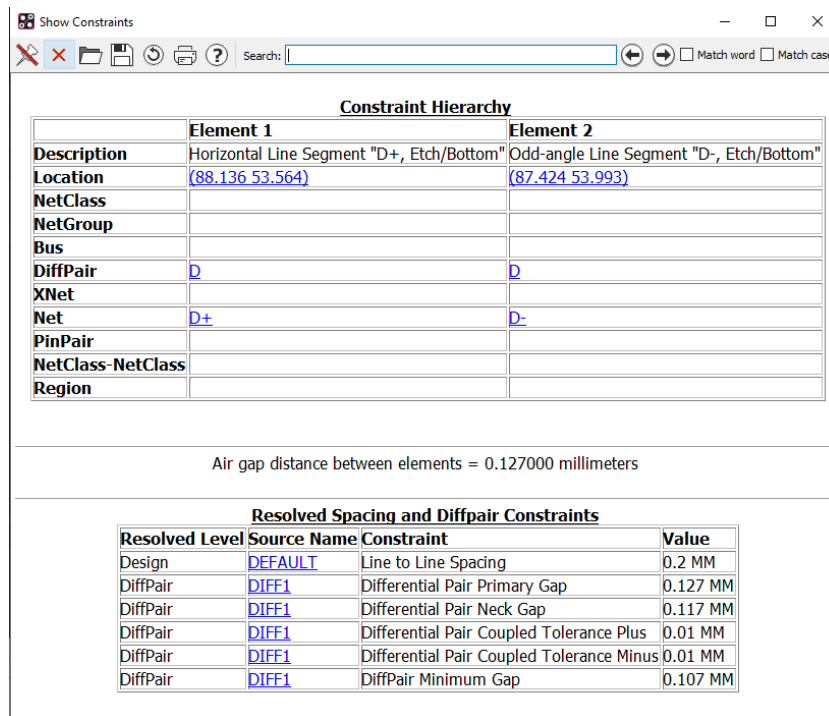
Objects			Referenced Physical CSet	Line 1
Type	S	Name		Min mm
*	*	*	*	*
Dsn		DEMOP-routed	DEFAULT	0.200
OType		Net Classes		
OType		Buses		
Bus		DATA[0..20](19)	DEFAULT	0.200
Bus		DATA1[0..9](10)	DEFAULT	0.200
Bus		DDS[0..10](11)	DEFAULT	0.200
Bus		MEMORY[0..29](30)	DEFAULT	0.200
OType		Diff Pairs		
DPr		CLOCK	DIFF1	0.127
DPr		D	DIFF1	0.127
DPr		DP_DATA0	DIFF1	0.127
DPr		DP_DATA1	DIFF1	0.127
DPr		DP_DATA2	DIFF1	0.127
DPr		DP_DATA3	DIFF1	0.127
DPr		DP1	DIFF1	0.127
DPr		STDA_SSRX	DIFF1	0.127
DPr		STDA_SSTX	DIFF1	0.127
OType		XNets/Nets		
Net		AEN/	DEFAULT	0.200
Net		A16	DEFAULT	0.200
Net		A17	DEFAULT	0.200

Constraint Resolution (All Levels)

You want to see how the constraint resolves between 2 objects?

Use Display > Constraint (Allegro) or Check > Constraints (OrCAD) then window select the 2 elements to obtain spacing resolution; select single element for physical resolution.

In the example below, I window selected the 2 clines of a Diff Pair to obtain spacing resolution. The actual measured gap is supplied in the middle section of the report.



Preventing Shorts (All Levels)

- ✓ In PCB Editor, It is possible to override a DRC with properties, make sure that the nets involved don't have the "NO_DRC" property on a pin(s).
- ✓ Make sure there are no "waived DRCs" that are not valid.
- ✓ Run DBDoctor to keep the design in sync and up to date.
- ✓ Make sure the plane layers in the cross section form agree with the artwork control form (negative or positive).
- ✓ Make sure the padstacks are designed properly; both Antipads and thermals
- ✓ Include the IPC-D-356 netlist in your Fab Package; insist the Fabricator does a netlist to Gerber compare.

Suppress SIGNOISE Warnings and Error messages (Allegro PCB Designer, OrCAD Professional)

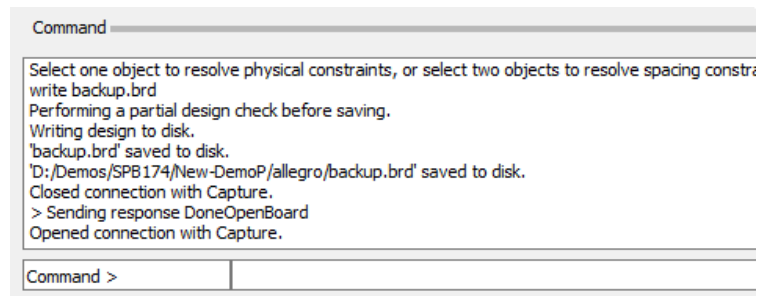
To suppress Signoise warning and error messages from appearing in the message window, set the variable in the env file.

set sigsuppress ERROR WARNING

Write vs Save (All Levels)

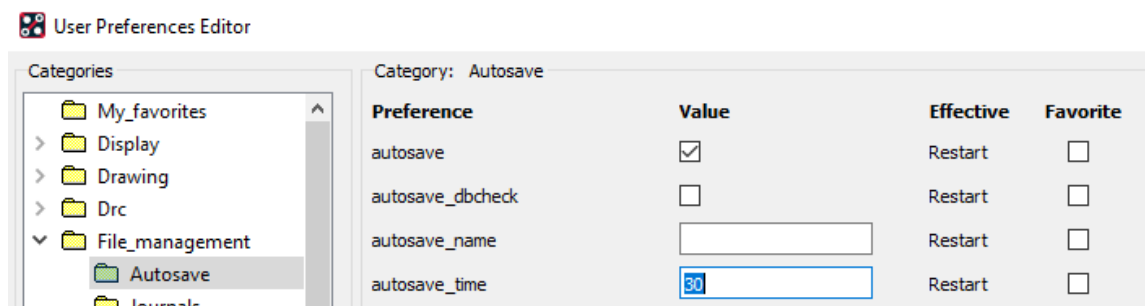
You want to save the current board file you are working on as a new name but want to keep the current file open using its current name. The "Save As" function will make the saved file the active file.

Enter "write" in the command window followed by a design name.



Autosave the Database (All Levels)

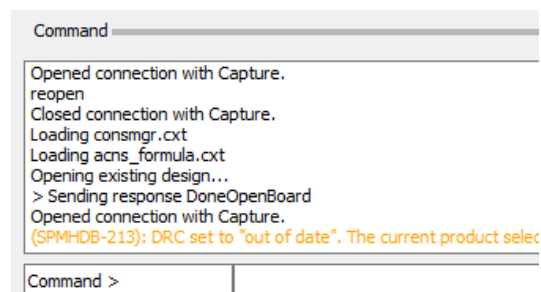
Setup > User Preferences > File_management > Autosave. Variables to autosave the database



Reopen command (All Levels)

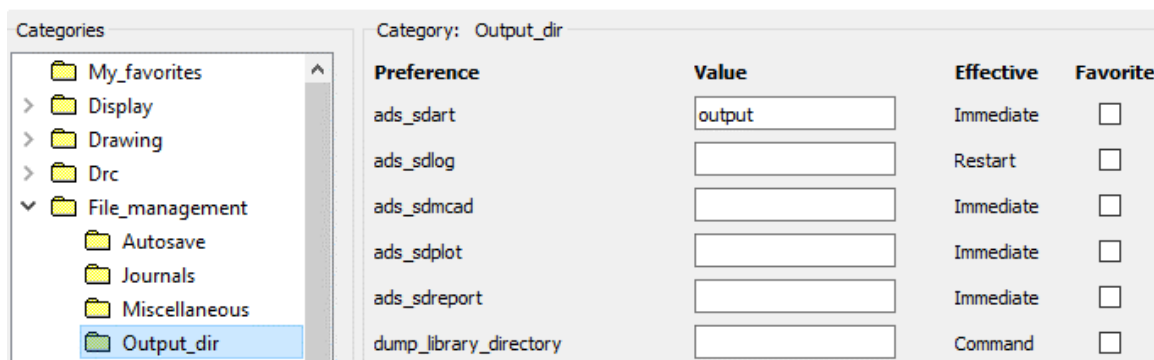
Most people do not know about this convenient command which does what it says, reopens a design file.

Enter “reopen” in the command window to reopen the same file.



File Management - artwork, plots, log files, reports (All Levels)

Looking to manage your artwork, plots and reports more efficiently? There is a suite of variables beginning with ADS designed to create subdirectories for common data files. Setup > User Preferences > File_management > Output_dir.



Open File Manager from Allegro (All Levels)

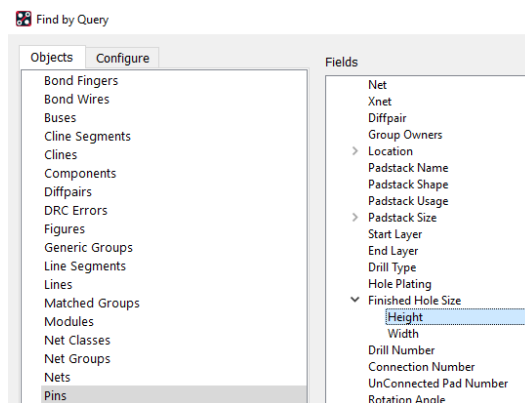
Quick method to explore to your working directory

Tools > Utilities > File Manager (Allegro) or Tools > More > File Manager (OrCAD).

Looking for a particular padstack based on hole size? (All Levels)

There are 2 methods to obtain a report of library padstacks:

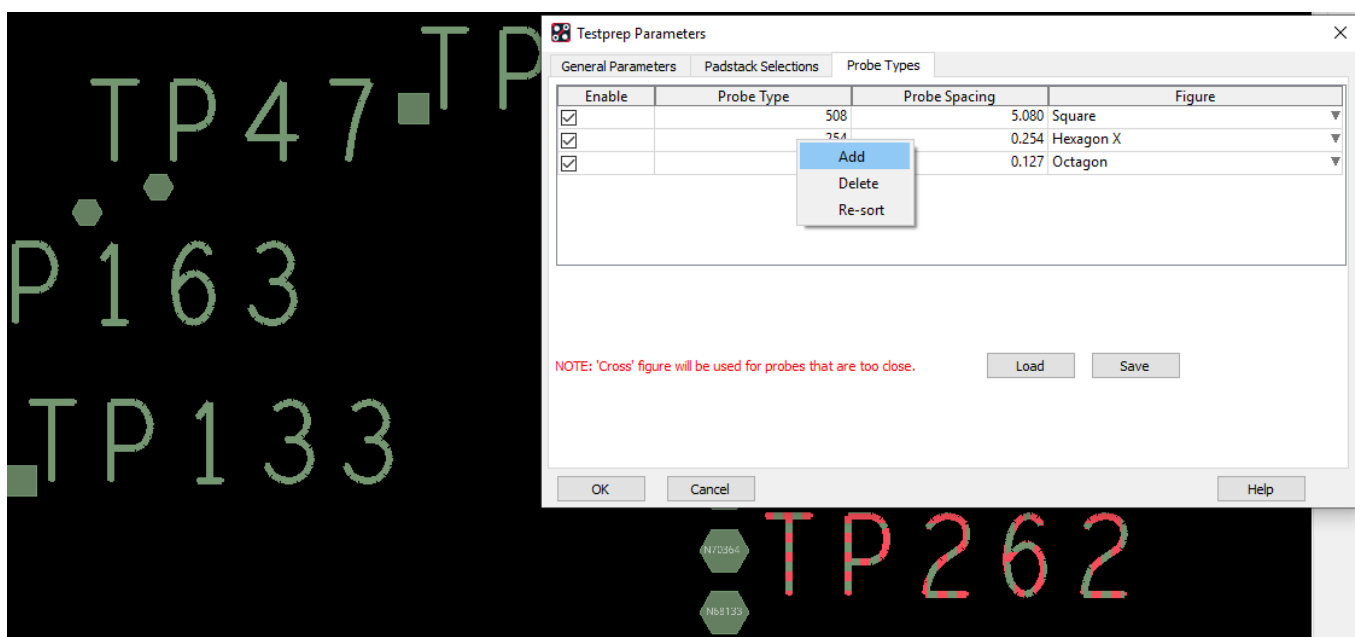
1. Manufacturing > NC > Drill Customization > Library Drill Report (Allegro) or Manufacture > Customise Drill Table > Library Drill Report (OrCAD).
2. Consider the Find by Query command available via the Find Pane. Set up a query to look for a particular Pin / via with a Finished hole size...



Testability – Multiple Probe-Type Support (All Levels)

The Testprep parameter form, Manufacture > Testprep > Parameters (Allegro) or Manufacture > Test points > Parameters (OrCAD) supports entries for multiple probe-types. The names (Probe Type) and centre to centre spacing (Probe Spacing) is user definable.

To add a row in the form, select a Probe Type cell then right click > Add.



Drill Legend Support for INCHES and METRIC (All Levels)

Update your default-units.dlt file as shown below (located normally %CDSROOT%\share\pcb\text\nclegend)

```
?AlternateUnits "millimeters"
?ColumnDefinitions '(
    ("Figure" "FIGURE" 7)
    ("Holesize" "SIZE" 15)
        ("Tolerance" "Tolerance" 15)
        ("Holesize2" "SIZE MM" 15)
    ("Tolerance2" "TOLERANCE MM" 15)
    ("PlateStatus" "PLATED" 10)
    ("NonStandard" "NONSTANDARD" 15)
    ("Quantity" "QTY" 6)
)
```

Uprev Symbols (All Levels)

The command “uprev_overwrite” can be used to uprev library files to the current software revision.

Syntax – uprev_overwrite n where n = *.dra; *.psm; *.ssm, etc

Ex – in a command window, enter uprev_overwrite *.dra to update all .dra files to the current software level.

For more flexibility in upreving in a DOS command window do a:

uprev -help

**** Be sure to make a backup copy of your library before uprev**

```

C:\>uprev_overwrite *.dra
0 warnings, 0 errors detected, 0 errors fixed.
Writing database to disk.
'cy2305.dra' saved to disk.
Done dbdoctor
Revising data for compatibility with current software.

Starting DBDOCTOR for drawing D:/work/marketing/Training/15.1/c_0603.dra
Checking db records
Checked 100 percent

0 warnings, 0 errors detected, 0 errors fixed.
Writing database to disk.
'c_0603.dra' saved to disk.
Done dbdoctor
Revising data for compatibility with current software.

Starting DBDOCTOR for drawing D:/work/marketing/Training/15.1/dip.dra
Checking db records
Checked 100 percent

0 warnings, 0 errors detected, 0 errors fixed.
Writing database to disk.
'dip.dra' saved to disk.
Done dbdoctor

```

Troubleshooting – Running Allegro in Safe Mode (All Levels)

Many Allegro programs support the "-safe" command line option. This starts the program without any user customizations or extensions. This can be used a debug mechanism to eliminate if user configurations are the cause of the problem with the product.

It disables loading at start-up

- local env file (%HOME%/pcbenv/env)
- cds_site configuration data
- any user skill code
- pre-register scripts
- ini file which stores window size/position information
- most recent used files (MRU)
- remembered Windows positions (.geo files)

In addition, graphic programs support the "-noopengl" option which will disable the enhanced Graphics based upon OpenGL.

Example: Run an "out of the box" allegro without opengl

```
allegro -safe -noopengl
```

Tips from Allegro PCB Users (All Levels)

Join the Cadence Community Website and see what other users are saying

https://community.cadence.com/cadence_technology_forums/f/pcb-design

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bottom symbol Pin number not visible in auto cad while exporting DXF file from allegro ?? started by kabalee on 4 Jan 2020 9:16 PM	3	243	By kabalee 20 Jan 2020 11:21 PM
NPTH HOLE NOT VISIBLE IN 3D VIEW (ORCAD PCB EDITOR17.X) started by GK MN on 20 Jan 2020 10:23 PM	0	32	By GK MN 20 Jan 2020 10:23 PM
VARIANT BOM started by Araugel on 20 Jan 2020 9:00 PM	0	32	By Araugel 20 Jan 2020 9:00 PM

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