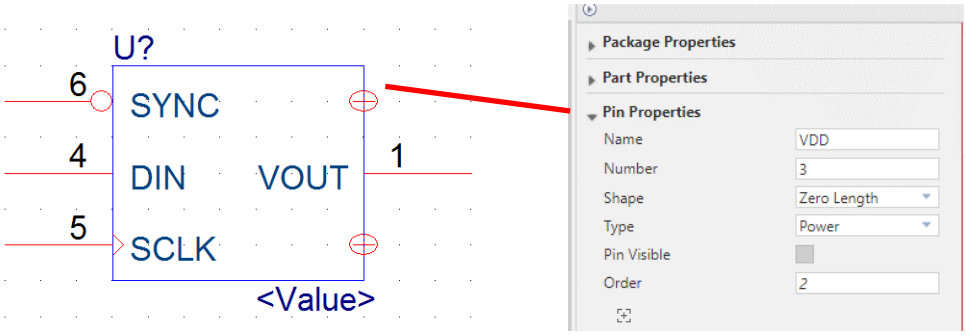
How to use Power Nets, Off Page Connectors, Global Signals and more….

OrCAD Capture offers users many ways to create their connectivity in a design. You can use net aliases (names), off page connectors, hierarchical ports and global symbols to make the connectivity required. There are some features which allow users the "control" over power nets and global signals which require some explanation. This App notes describes the different methods for power connectivity in OrCAD Capture.

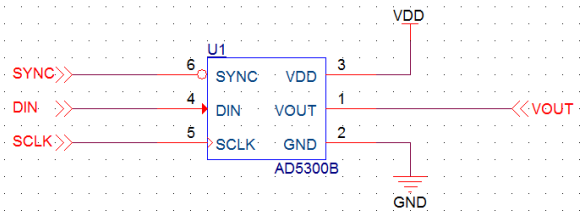
Invisible Power Pins

By default many of the OrCAD Capture symbols provided use the invisible power pin. This is a pin that is of type POWER but is not visible on the schematic symbol. The Pin Name is used to connect like named pins together. This feature can assist in "de-cluttering" the schematic canvas. You can control the pin type, visibility, name and number when the pin is added during symbol creation

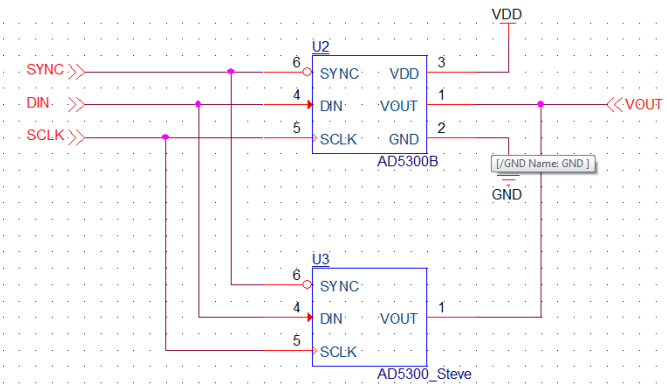


The example below shows two parts on one design page and another on a different page of a design, two symbols U1 and U2 use the visible power pin for GND and VDD connected via a global power symbol and U3 has invisible power pins that are named VDD and GND.

Page 1



Page 2



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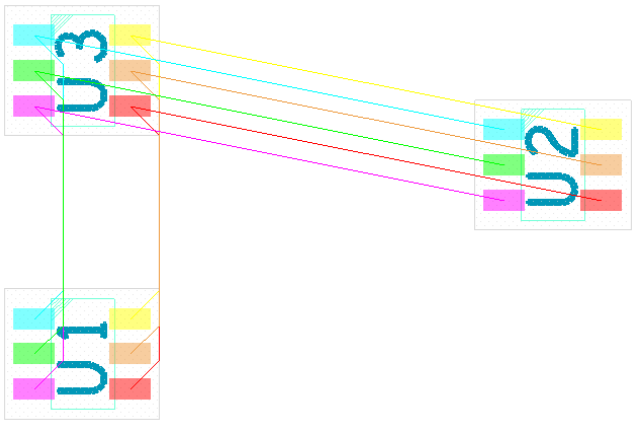
The resulting design sync, once in PCB Editor (OrCAD or Allegro) results in full connectivity between all three IC's.



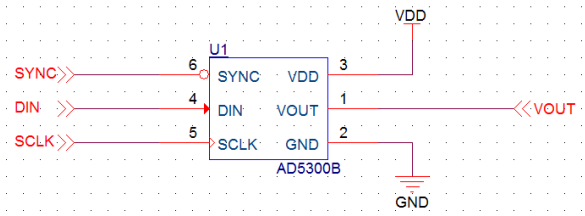
Colour code for reference:-
Blue – VOUT
Green – GND
Pink – VDD
Red – DIN
Orange – SCLK
Yellow – SYNC

The Off Page connectors create connectivity between page 1 and page 2 at the same level of hierarchy, the global symbols provide connectivity across the whole design (unless you take control). The Invisible Power Pins connect to the same netname as the power symbols because the pin names match the global power symbol name, i.e. GND or VDD.

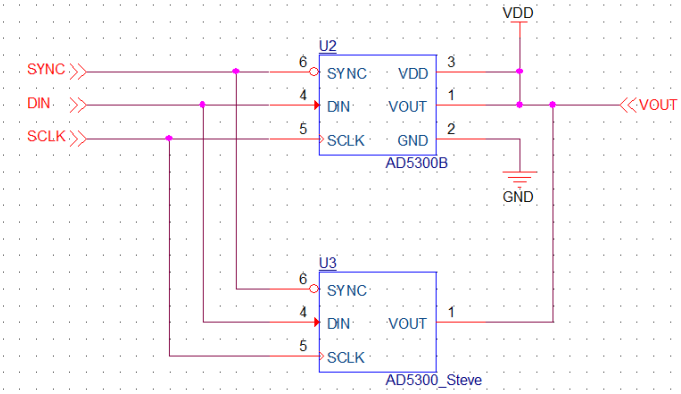
Taking control of Global Power Symbols using Off-Page Connectors

In some instances users will want to take over the control of a global power signal. This may be for hierarchical reasons where a user needs a local GND signal and wants to join them at a certain location. To do this, users need to connect the power signal in question to either an off-page connector or a hierarchical port. As soon as this takes place then the name of the port or off page connector becomes the "winning" netname value. In the example below page 1 remains as it did in the first example but page 2 has the VOUT net pulled high. Although both VDD and VOUT are displayed and visible the "winning" netname value would match the off-page connector name of VOUT.

Page 1



Page 2



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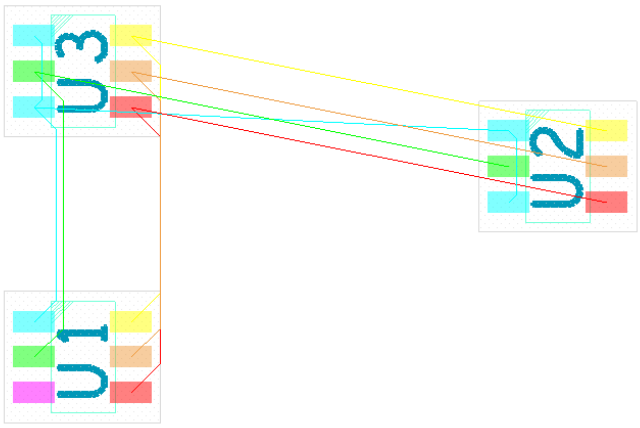
The resulting design sync, once in PCB Editor (OrCAD or Allegro) results in full connectivity between all three IC's but this time you can see that VOUT has consumed the VDD net for U2 and U3 (both page 2) but not for U1 which is on page 1 the net name remains as VDD so is now a single node net.

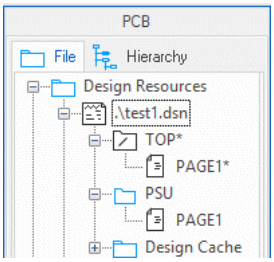


Colour code for reference:-
Blue – VOUT
Green – GND
Pink – VDD
Red – DIN
Orange – SCLK
Yellow – SYNC

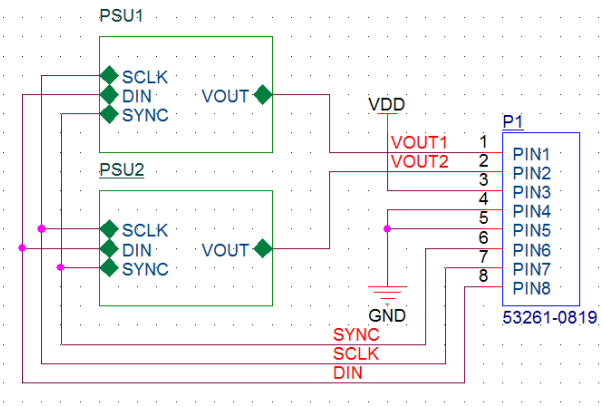
This type of occurrence is rare because you normally would not use an off-page connector in this type of design. You would normally rely on the off-page connectors for general net names and use power symbols for the power nets, VDD, GND etc.

Taking control of Global Power Symbols using Hierarchical Ports

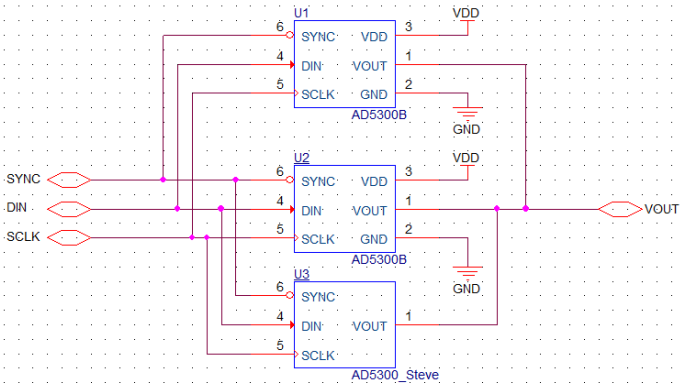
In this next example we add hierarchy to the design. There are many advantages to using hierarchy in a design, especially if you have multiple instances of the same schematic block you can draw this item once and then use the hierarchy to control the multiple instances. This also allows you to control the power symbols inside each hierarchy. The first instance takes our existing design simplified now all on page 1 of a separate schematic folder called PSU. There is also now a new schematic folder TOP that contains 2 blocks of the same circuit, PSU1, PSU2. Initially we use the same VDD and GND for both blocks using a global power symbol.



Page 1 (TOP of the hierarchy)



Page 2 (PSU repeated twice, PSU1 and PSU2)



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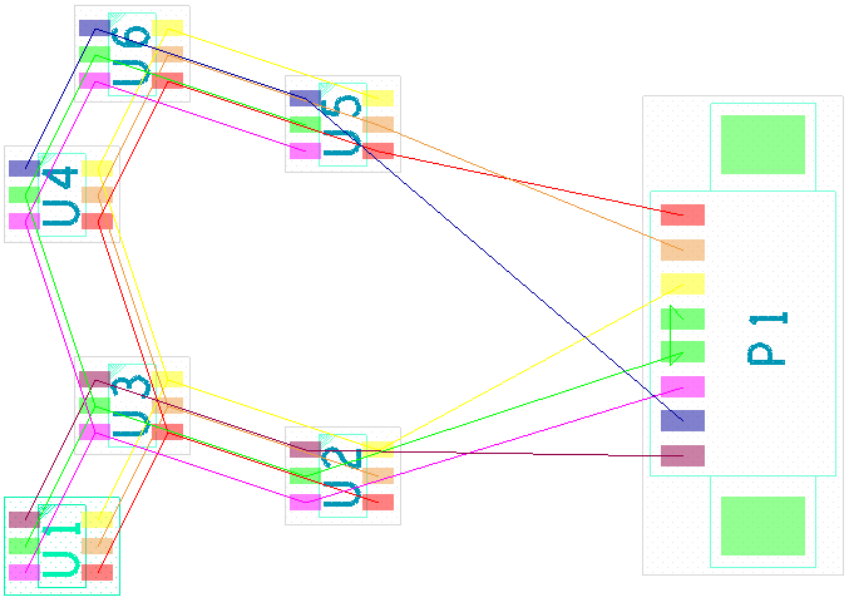
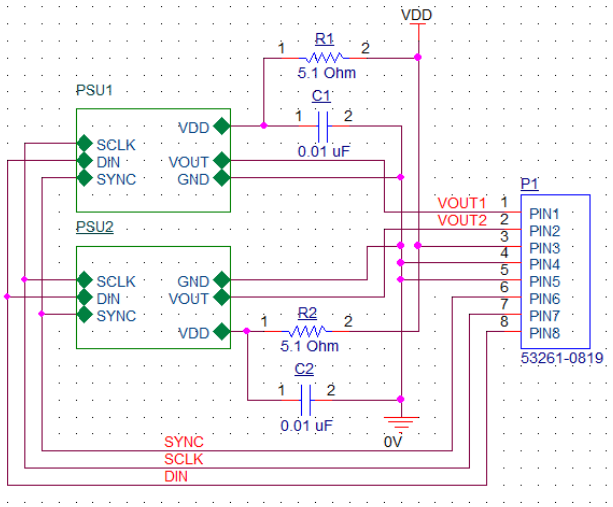
The resulting design sync, once in PCB Editor (OrCAD or Allegro) results in full connectivity between all six IC's and the connector. The connectivity matches the hierarchical ports and the global power symbols.



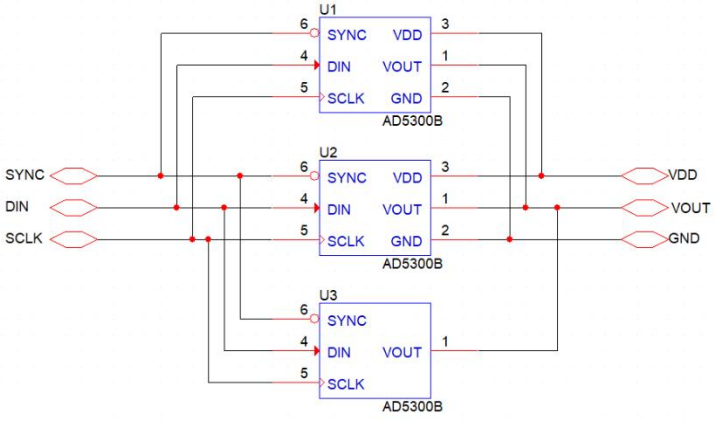
Colour code for reference:-
Blue – VOUT1
Brown – VOUT2
Green – GND
Pink – VDD
Red – DIN
Orange – SCLK
Yellow – SYNC

If we now join the global power symbols to hierarchical ports we again take control of the power net names. This might be useful if you want separate POWER signals for each block. In the next example we have connected the VDD and GND to a hierarchical port. These are then connected to an R C arrangement. The GND net is connected to 0V at the top level. This is the "winning" value because it's at the Top of the hierarchy. You can also see that VDD is connected to either side of the resistors.

Page 1 (TOP of the hierarchy)



Page 2 (PSU repeated twice, PSU1 and PSU2)



If we now design sync, now are the results as expected? Yes. The 0V is the winning net name value so has consumed the GND at the lower level and 0V is now the net name on the design. The VDD is still connected but only at the top level (P1, R2 and R2). The other end of the two resistors has taken the unnamed net name from the connection at the top level (auto-generated names N02679 and N03182) In these instances it would be better to name the net at the top level something intelligent so we can recognise the names we require once we get to the PCB stage,

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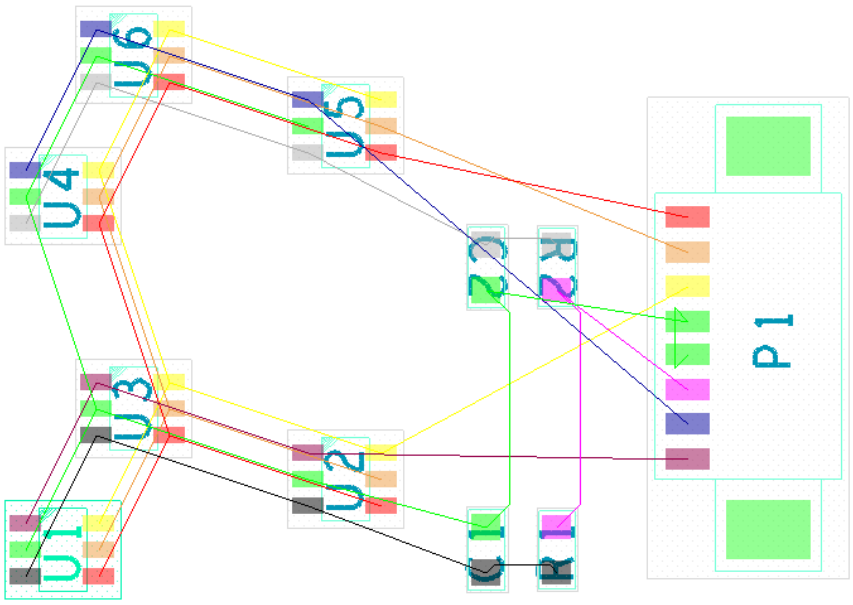

Colour code for reference:-
Blue – VOUT1
Brown – VOUT2
Green – GND
Pink – VDD
Red – DIN
Orange – SCLK
Yellow – SYNC
Black – N02679
Grey – N03182

Adding Hierarchical Ports at the Top of the hierarchy

Some users will use hierarchical ports regardless of whether there is a design reason or not, mainly because of the graphical appearance. If this is done and the design is hierarchical, ports added to the root schematic can have adverse effects on the connectivity within the design. It would be better to design a new off-page connector that gives the required symbol appearance. Use the New symbol function or copy an existing off-page connector and modify accordingly.

Summary

Another suggestion for net names is to just add a net alias to the wire. If you have the same net alias on the same page then this will connect. As soon as you want this to connect across pages then you MUST use an off-page connector or hierarchical port. Global symbols connect across the whole design UNLESS you connect them to an off-page connector or hierarchical port whereby you then take control.

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