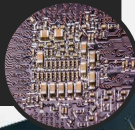


# Cadence Next Generation Solutions

# System Design Must Advance with Industry Demands

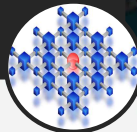
Smaller, Faster, Cheaper



Remove Bottlenecks & Increase Throughput



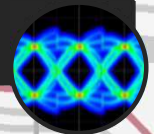
Solutions that Scale Required



More Work Fewer Resources



Actionable Analysis Required

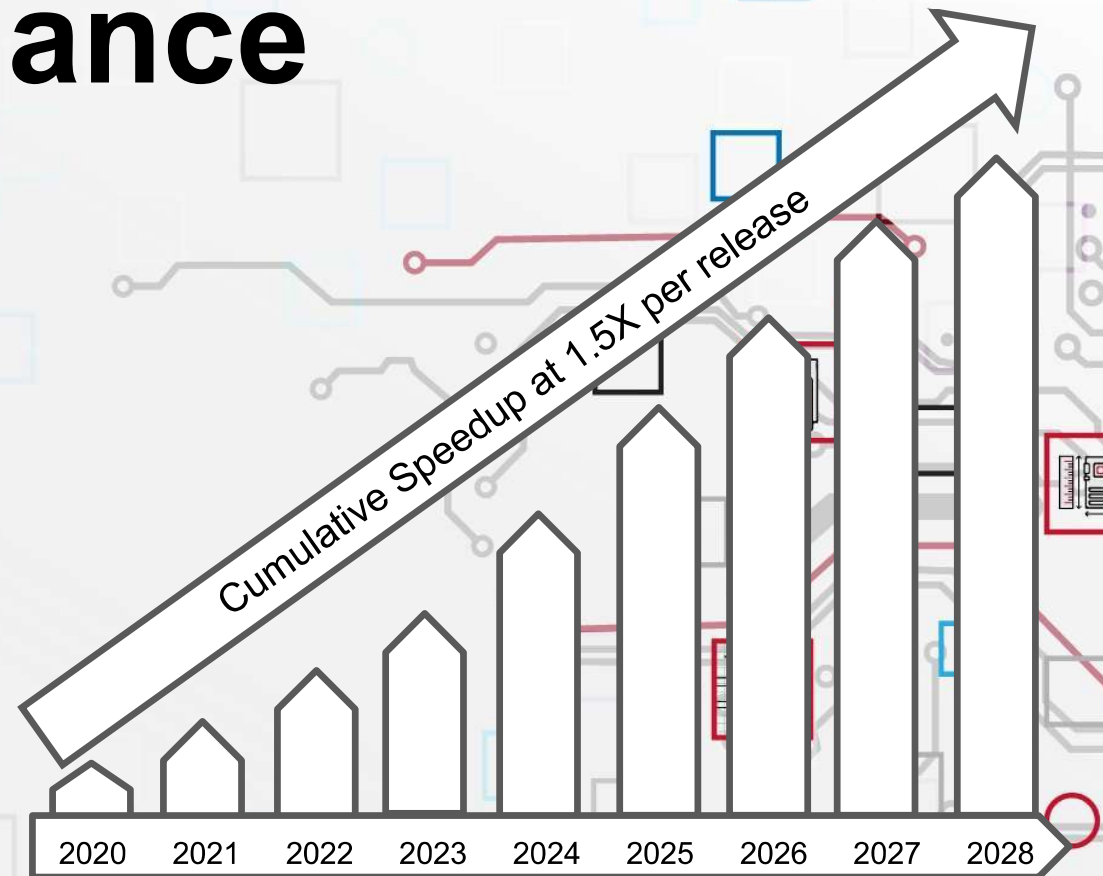


In-Context Data Connectivity & Insights Needed



# Pure Performance

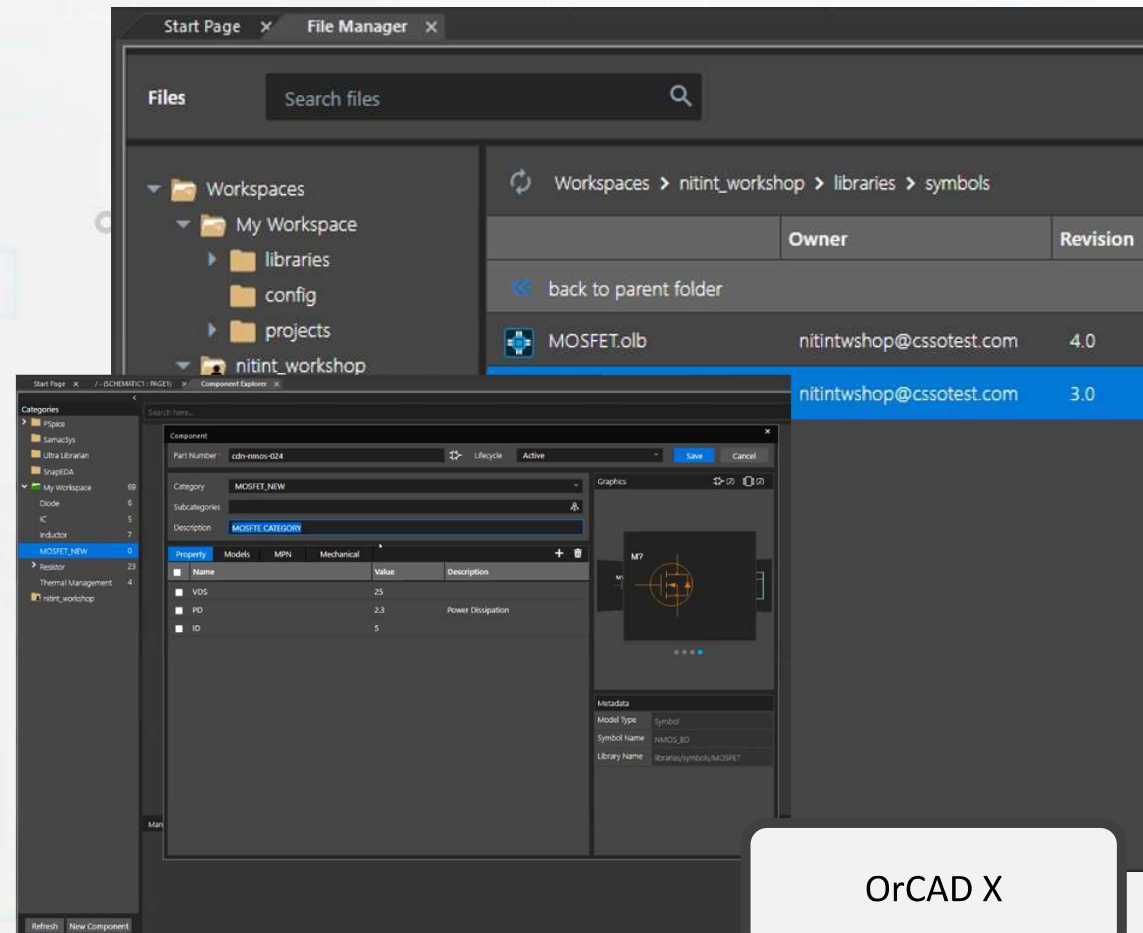
- Allegro® X performance acceleration
  - 10X+ faster interactive shapes
  - General GPU - 20X+ faster rendering
  - PSpice 5X faster
- 40X+ faster 3D engine; Up to 20X reduction in process memory
- Smaller memory footprint



*Creating Leading Performance and Capacity  
→ Compounding is 8<sup>th</sup> Wonder of the World*

# Cloud Workspaces

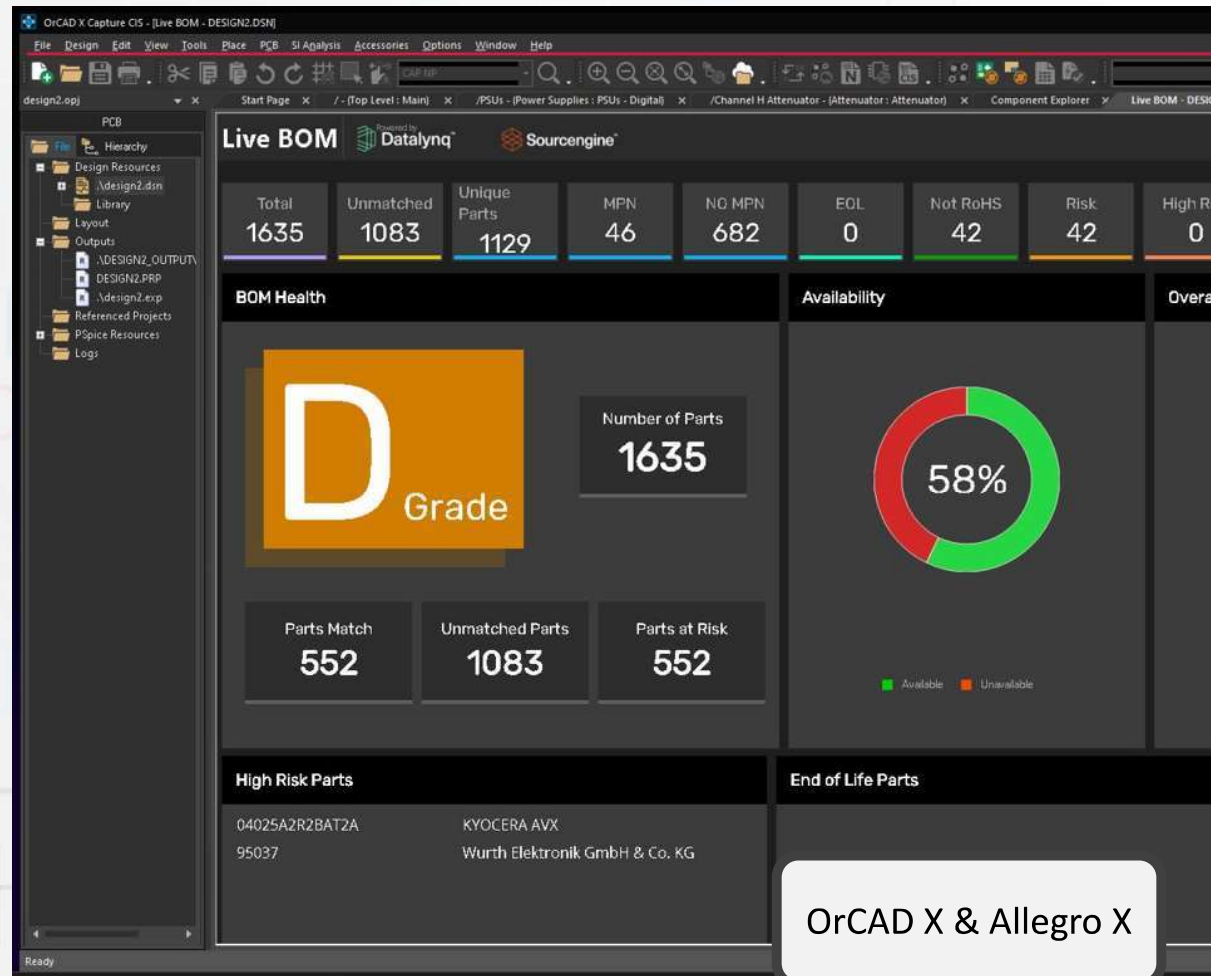
- Cadence Cloud Repository
- Store and share design files and libraries
- No setup and config required



OrCAD X

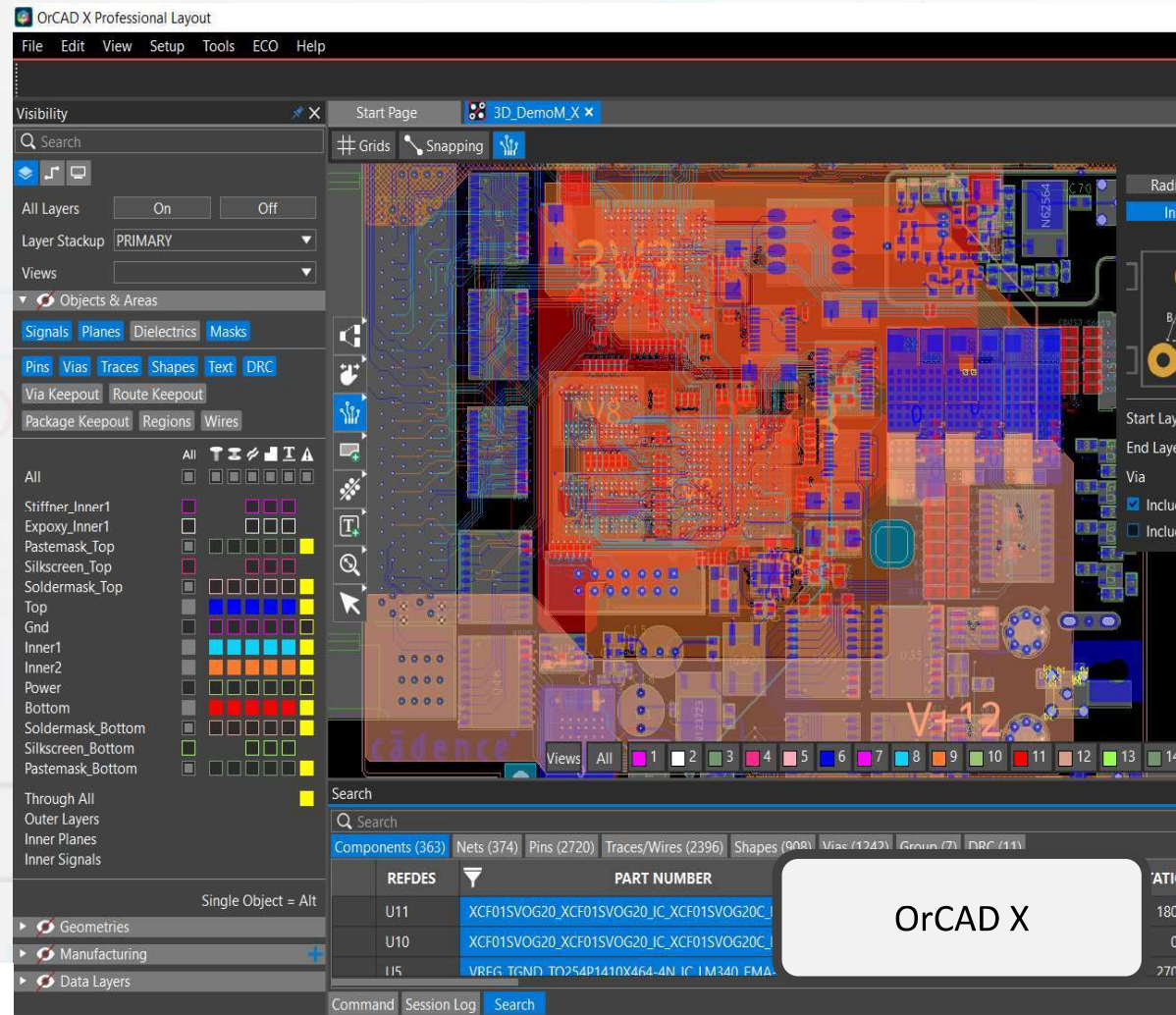
# LiveBOM

- On-demand supply chain intelligence
- Reviews active design and provides a grade
- Swap and update parts quickly as needed
- Ensure a compliant and orderable BOM
- Powered by SourceEngine



# Presto

- New PCB Layout UX
- Focused on productivity & ease of use combined with powerful layout and routing engines of Allegro
- Great for new and occasional designers
- Fully compatible with OrCAD & Allegro PCB Editor (same .brd)
- Optional. Evaluate and leverage at your pace



OrCAD X

# Presto

- Use model and UI overhaul
- Designed to make information discoverable, data presentation contextual
- Live links to drill into details where applicable
- Built-in search engine with live editing
- Visual help and guidance

**Search & Modify**

OBJECT	LAYER	NET	WIDTH	X LOCATION	Y LOCATION	GROUP	ASSOCIATED REFDES	PROFILE	VERSION	DIAMETER
Trace	Sig_6H	1394_PLL	4.00	8455.91	3412.20					
Trace	Sig_6H	1394_TSD_IN_CLK	4.00	8022.83	3687.80					
Trace	Sig_6H	1394_TSD_IN_DATA	4.00	8022.83	3569.69					
Trace	Sig_6H	1394_TSD_IN_SYNC	4.00	8022.83	3648.43					
Trace	Top	+0.75V	3550	407.28	8875.00					

**Graphical Guidance**

Radial

In Out In/Out

Trace Width (A)

Constraint

Channel Space (B)

10.000

Pin-Via Space (C)

5.000

Start Layer Top

End Layer Bottom

Via Net Default

Include Unassigned Pins

Include All Same Net Pins

**Configurable R2M Packaging**

IPC:

- PCB Design Report
  - Summary Report
  - Unconnected Pins Report
  - DRC Report
  - Etch Length Report
  - Database Diary Export
- IPC2581 Database (Fabrication)
- Livedoc Fabrication and Assembly Docume
- Livedoc Fabrication and Assembly PDF
- IPC2581 Database (Fabrication)
- IPC-2581
  - IPC2581 Database (Fabrication)
  - IPC2581 Database (Assembly)
  - Artwork

**Live DRC Panel**

Sha 134

Unassigned Shapes 0

Out of Date Shapes 0

DRC Up to Date

Design(13)

Electrical(24)

Physical(6)

Spacing(21)

DRC Errors 64 Shorting Errors 8

Waived Errors 0 Waived Shorting Errors 0

Highlight DRC on Canvas

**Contextual Help**

Shape Utiliti

Resize Boolean Trim Corners

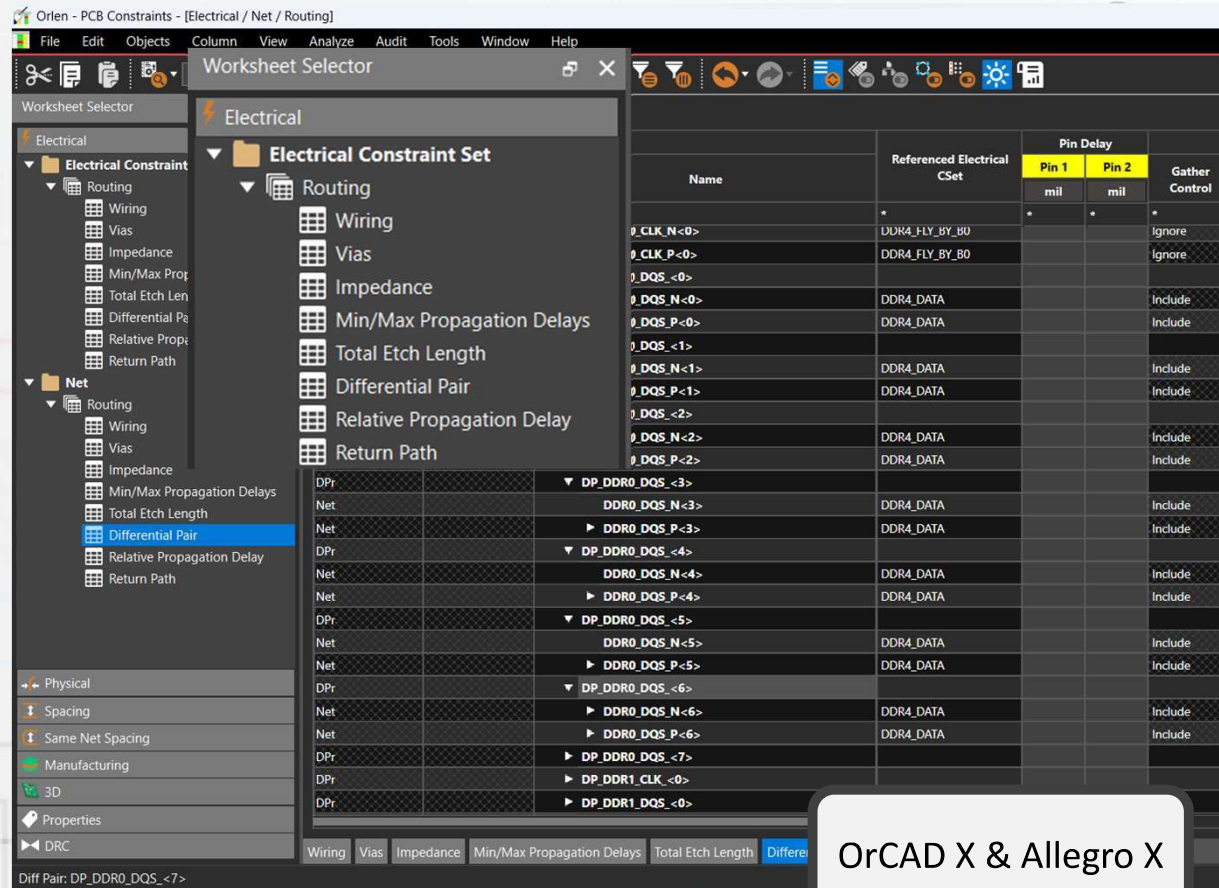
Merge Intersect Subtract Exclude

Select Reference Shape

**OrCAD X**

# Shift-Left: Expanded Constraints

- Full constraints at all levels
- View and set rules regardless of tier
- Ensure correct by construction design



The screenshot displays the 'Electrical Constraint Set' configuration in the software. The 'Routing' folder is expanded, showing various constraint types like Wiring, Vias, Impedance, etc. A table on the right lists specific constraints with their referenced electrical CSet and pin delay settings.

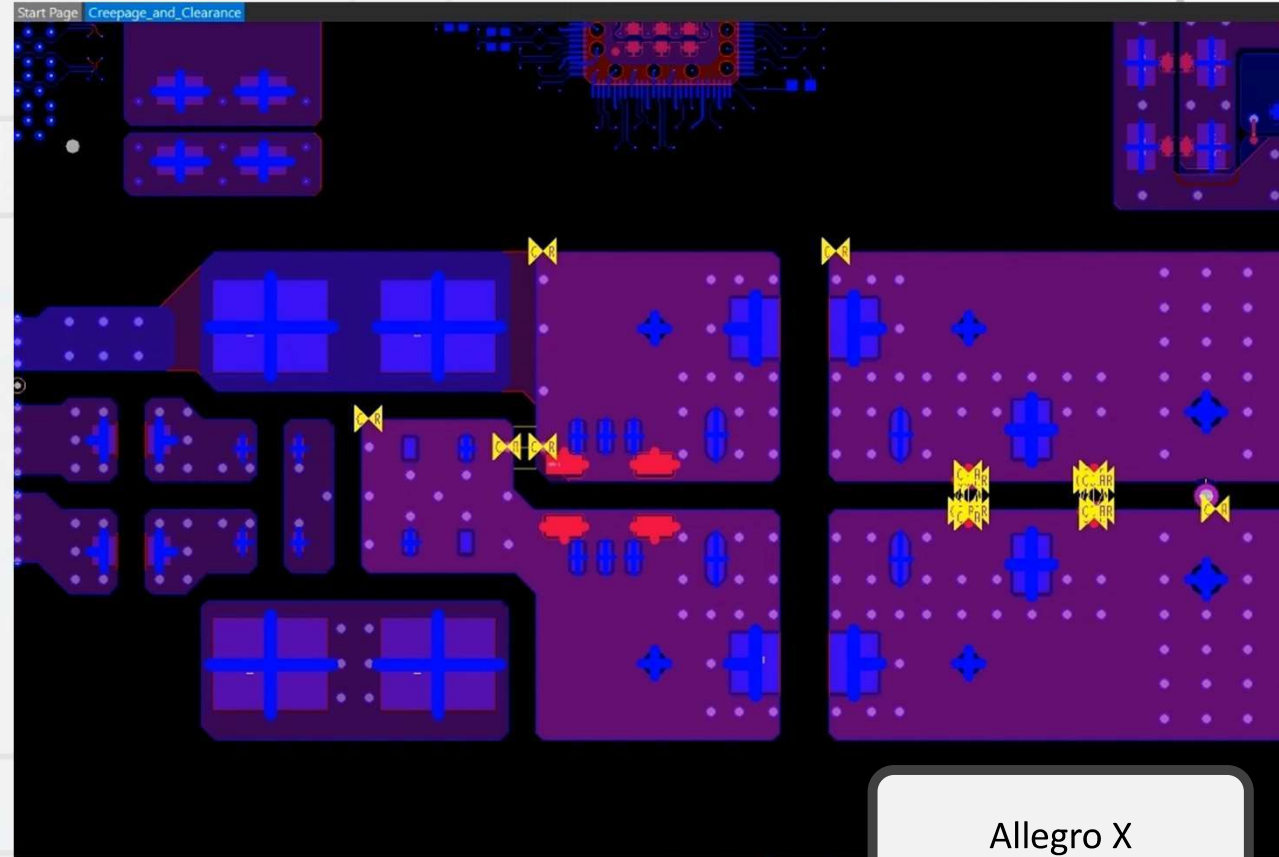
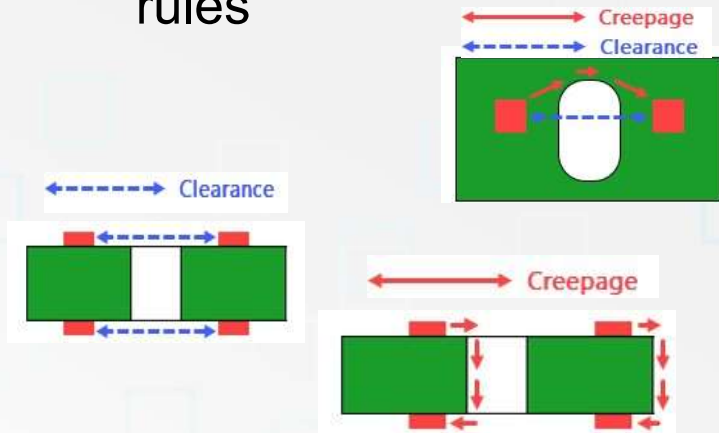
Name	Referenced Electrical CSet	Pin Delay		Gather Control
		Pin 1 mil	Pin 2 mil	
# CLK_N<0>	DDR4_FLY_BY_B0	*	*	Ignore
# CLK_P<0>	DDR4_FLY_BY_B0			Ignore
# DQS_<0>				
# DQS_N<0>	DDR4_DATA			Include
# DQS_P<0>	DDR4_DATA			Include
# DQS_<1>				
# DQS_N<1>	DDR4_DATA			Include
# DQS_P<1>	DDR4_DATA			Include
# DQS_<2>				
# DQS_N<2>	DDR4_DATA			Include
# DQS_P<2>	DDR4_DATA			Include
DPr				
Net	DDR0_DQS_N<3>			Include
Net	DDR0_DQS_P<3>			Include
DPr				
Net	DDR0_DQS_N<4>			Include
Net	DDR0_DQS_P<4>			Include
DPr				
Net	DDR0_DQS_N<5>			Include
Net	DDR0_DQS_P<5>			Include
DPr				
Net	DDR0_DQS_N<6>			Include
Net	DDR0_DQS_P<6>			Include
DPr				
Net	DDR0_DQS_N<7>			Include
DPr				
DPr				

OrCAD X & Allegro X



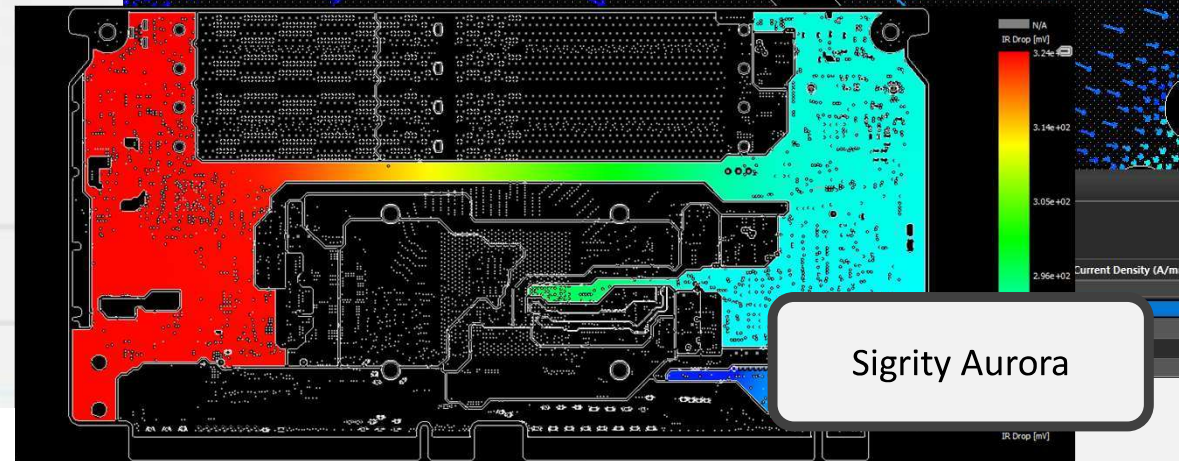
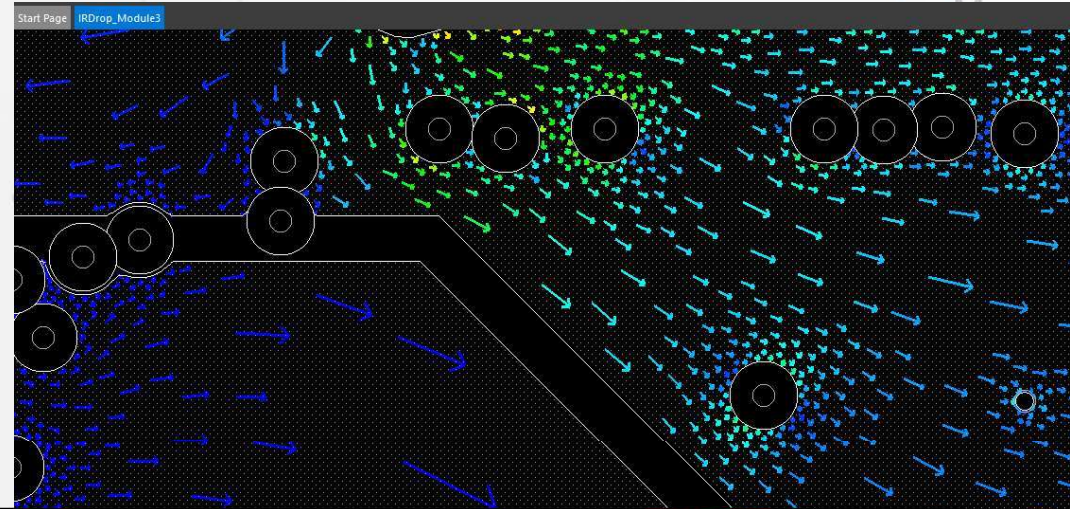
# Shift-Left: Expanded Constraints

- New high-voltage constraint checks to verify Creepage and Clearance rules



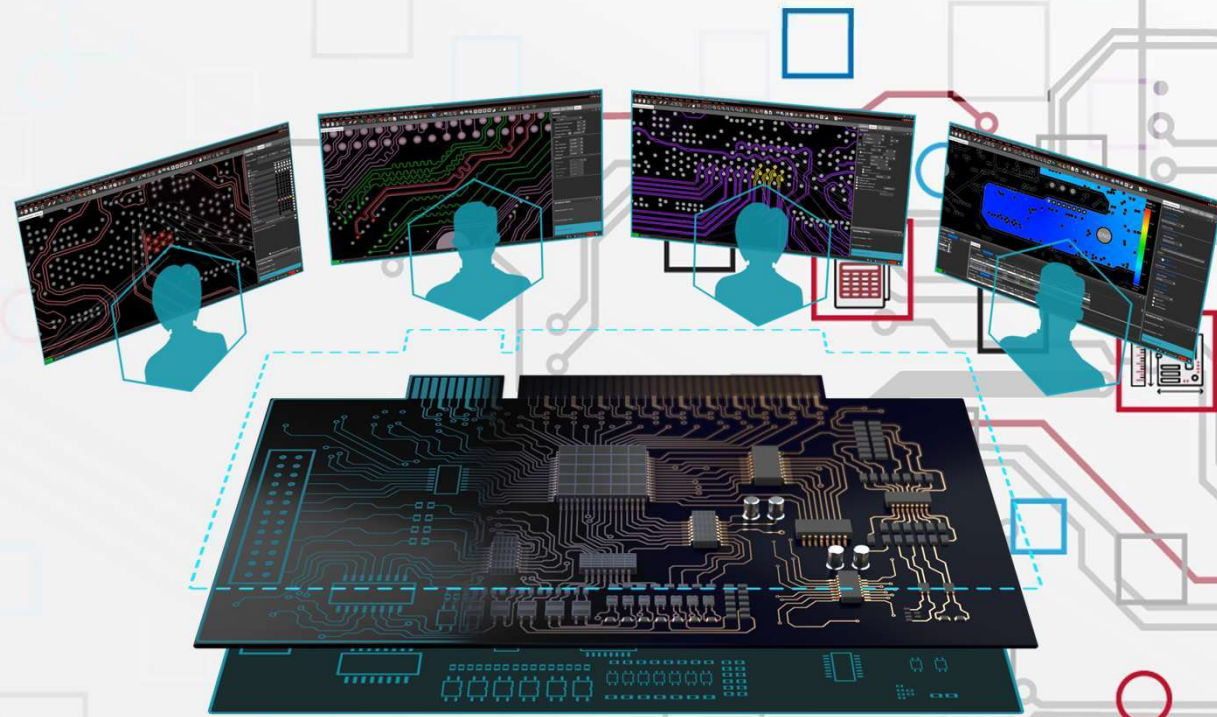
# Shift-Left: In-Design Analysis

- Perform electrical analysis inside the design canvas
- Visual overlays make finding and fixing issues quick & effective
- Analysis to cover:
  - Impedance
  - Coupling
  - IR Drop
  - Crosstalk
  - Return path
  - Thermal (coming soon)



# Symphony

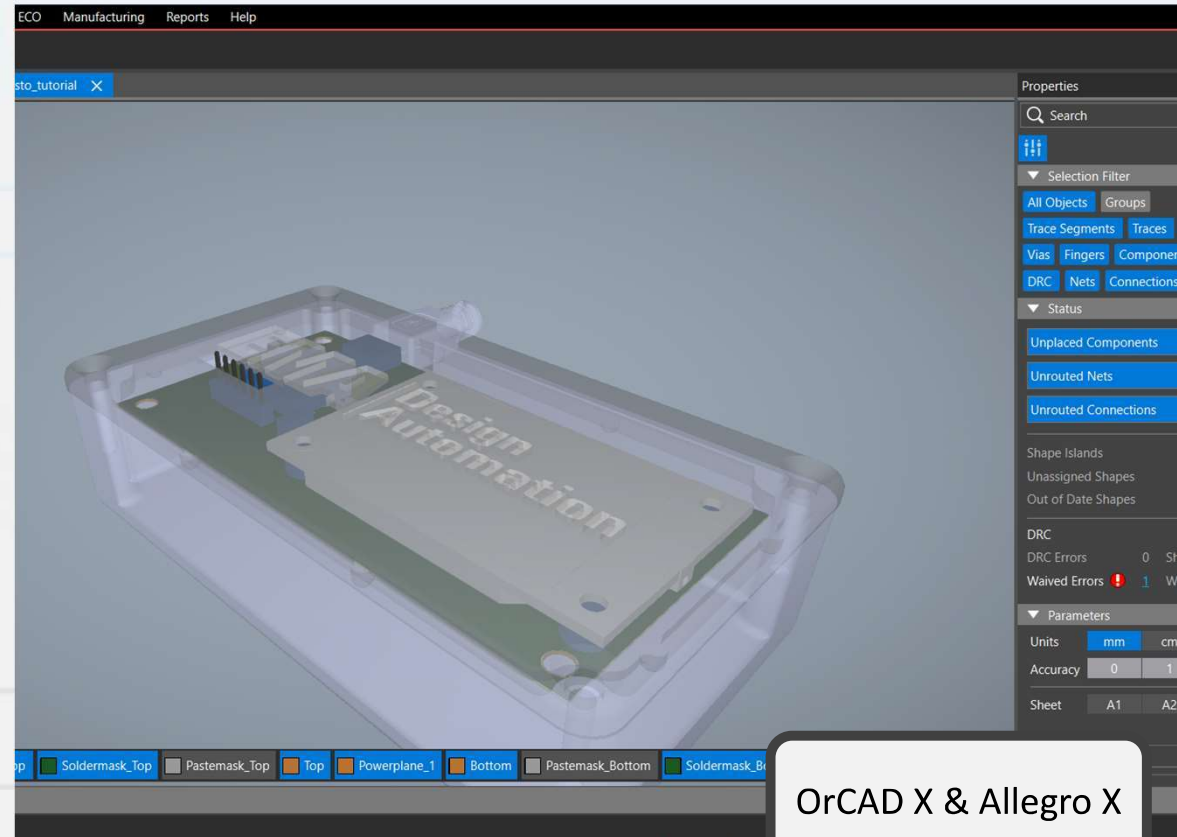
- Concurrent PCB design
- Multiple models (cloud, adhoc, hosted server)
- 2 or more can design and edit at the same time
- Ability to include simulation with Aurora
- 2 person included in OrCAD X Pro



OrCAD X & Allegro X

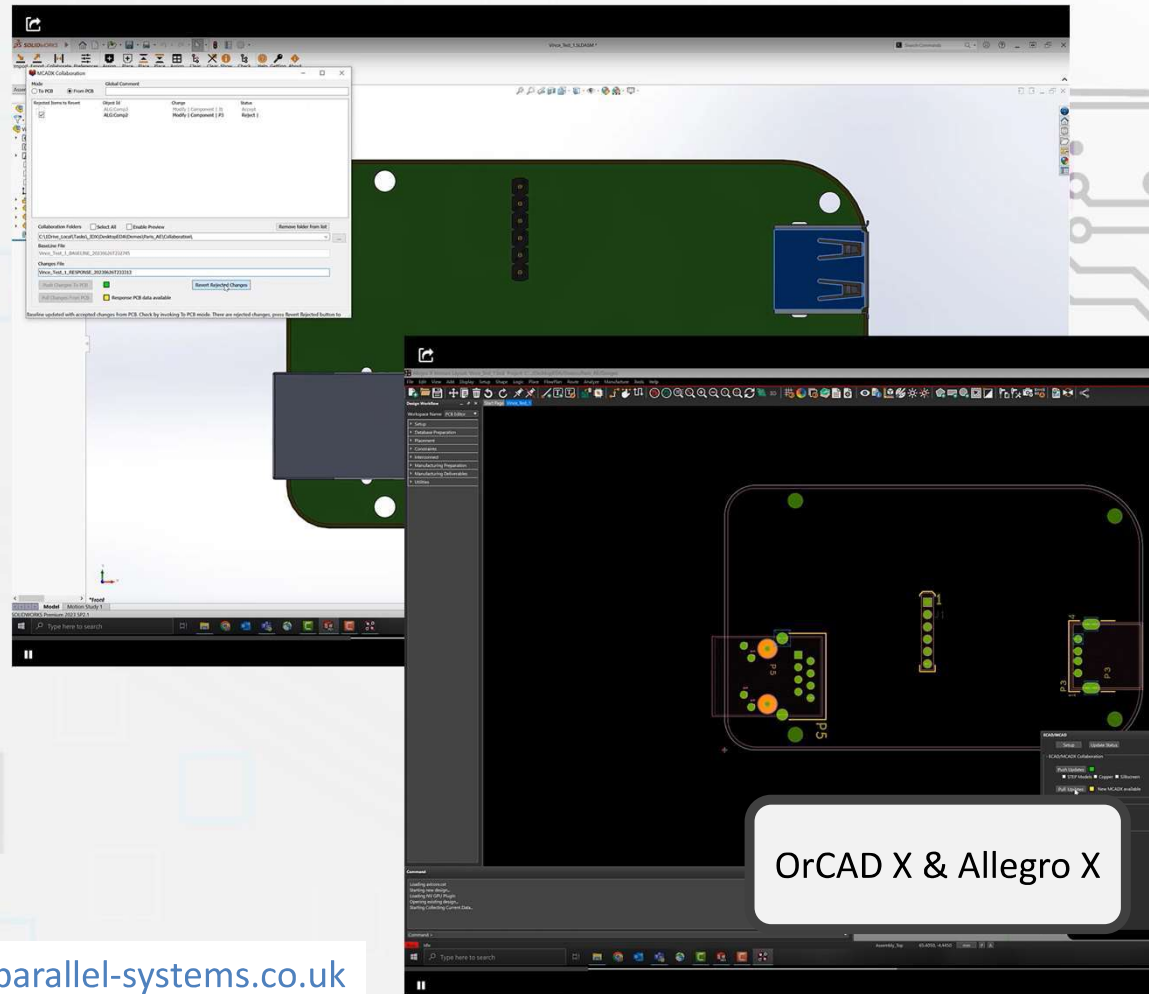
# New 3D Engine

- New 3D engine
- Built for performance
- Real-time 3D constraints
- Import mechanical elements – export design for mechanical integration



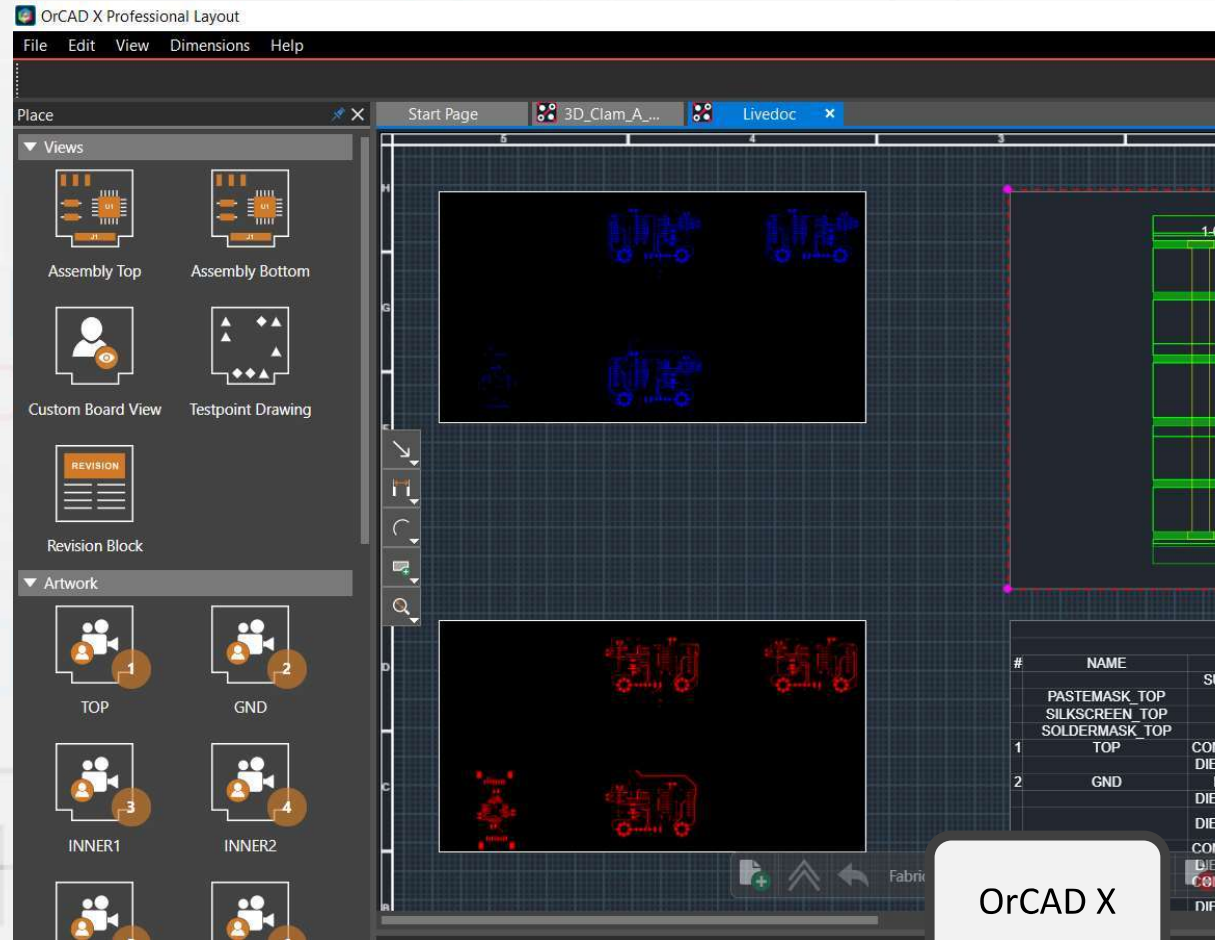
# MCAD X

- ECAD/MCAD Collaboration
- Incremental updates with accept / reject, commenting, and history tracking
- For SOLIDWORKS first
- Make ECAD/MCAD easier to do and happen more often



# LiveDoc

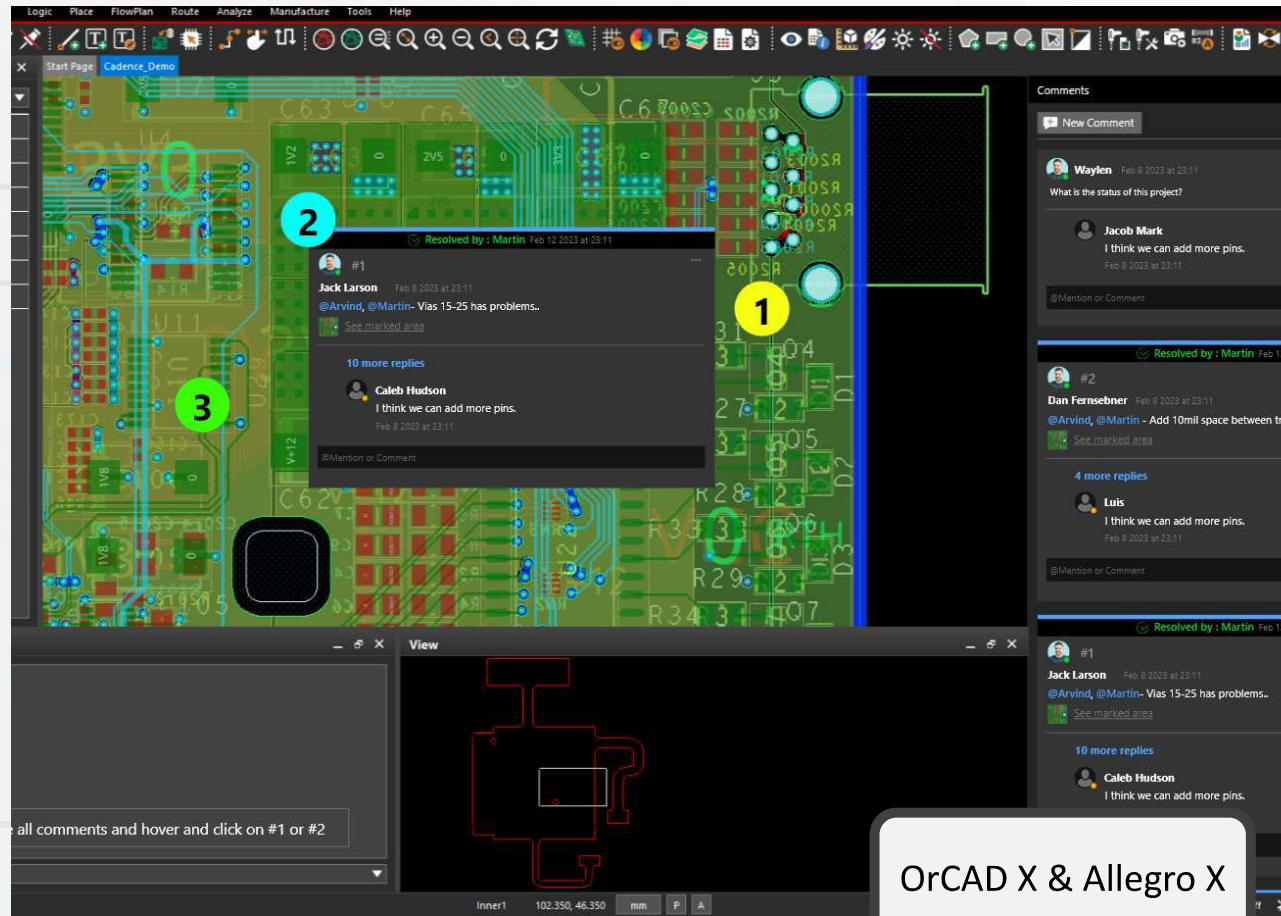
- Automated PCB Documentation
- Live Updates
- Template Driven
- Ensure docs are complete, up to date and ready



OrCAD X

# Review & Markup

- Embedded Markup Layer
- Like GoogleDocs
- Stored in PCB database
- Commenting, Resolve, history tracking



# X Platform Benefits

- ✓ Reduce late-stage errors – shift problem solving left
- ✓ Enable proactive problem solving
- ✓ Enable early analysis & optimization
- ✓ Increase engineer efficiency
- ✓ Increase schedule predictability & accuracy



# Cadence Leadership in AI

*Targeting the Next 10X in Productivity Improvement*

**Xcelium™ ML**  
Regression Simulation

**Optimality™**  
In-Design Optimization

**Verisium™**  
Verification

**Cerebrus™**  
Digital Implementation

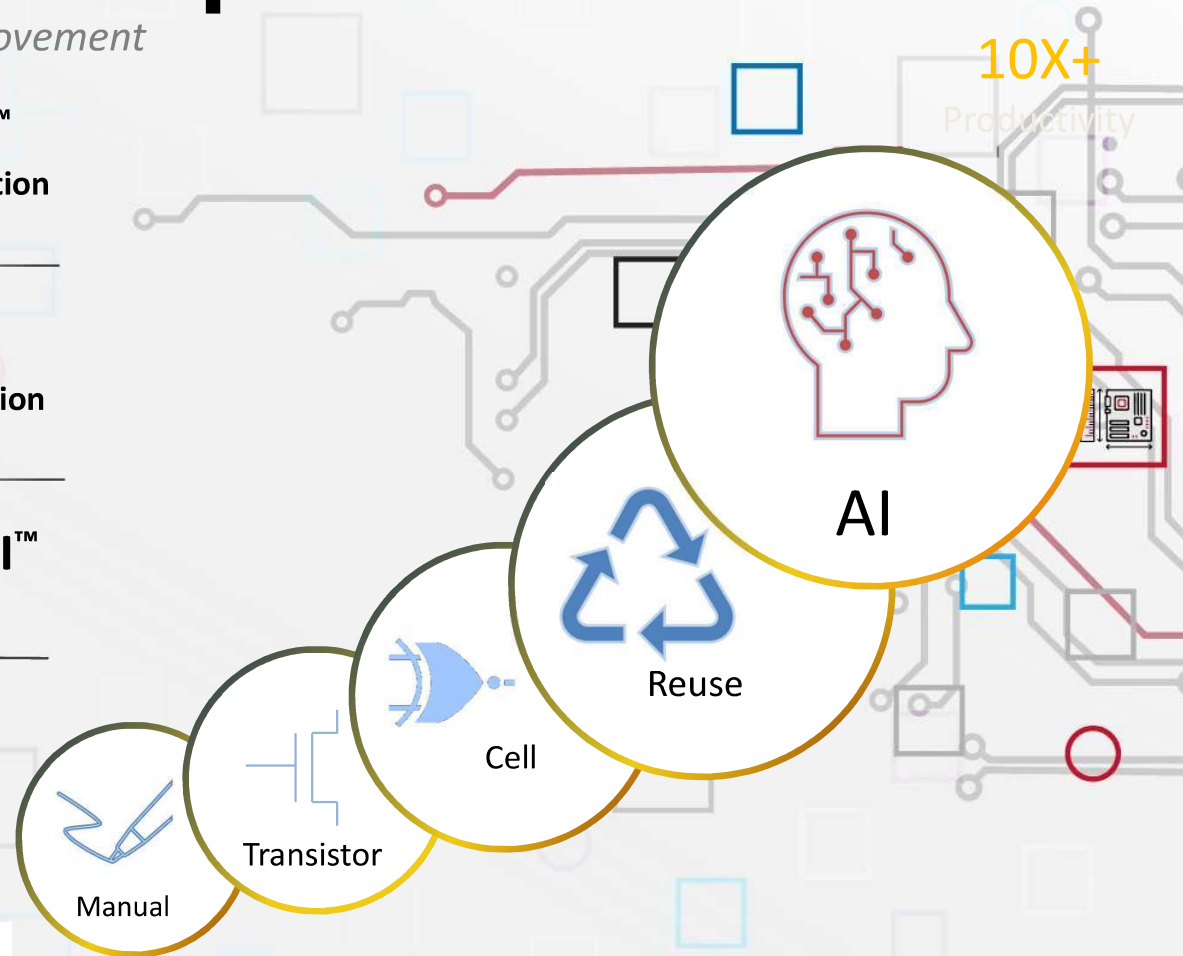
**Virtuoso Studio™**  
Custom and Analog Design

**Allegro X AI™**  
PCB

**JedAI**  
Joint Enterprise Data AI Platform

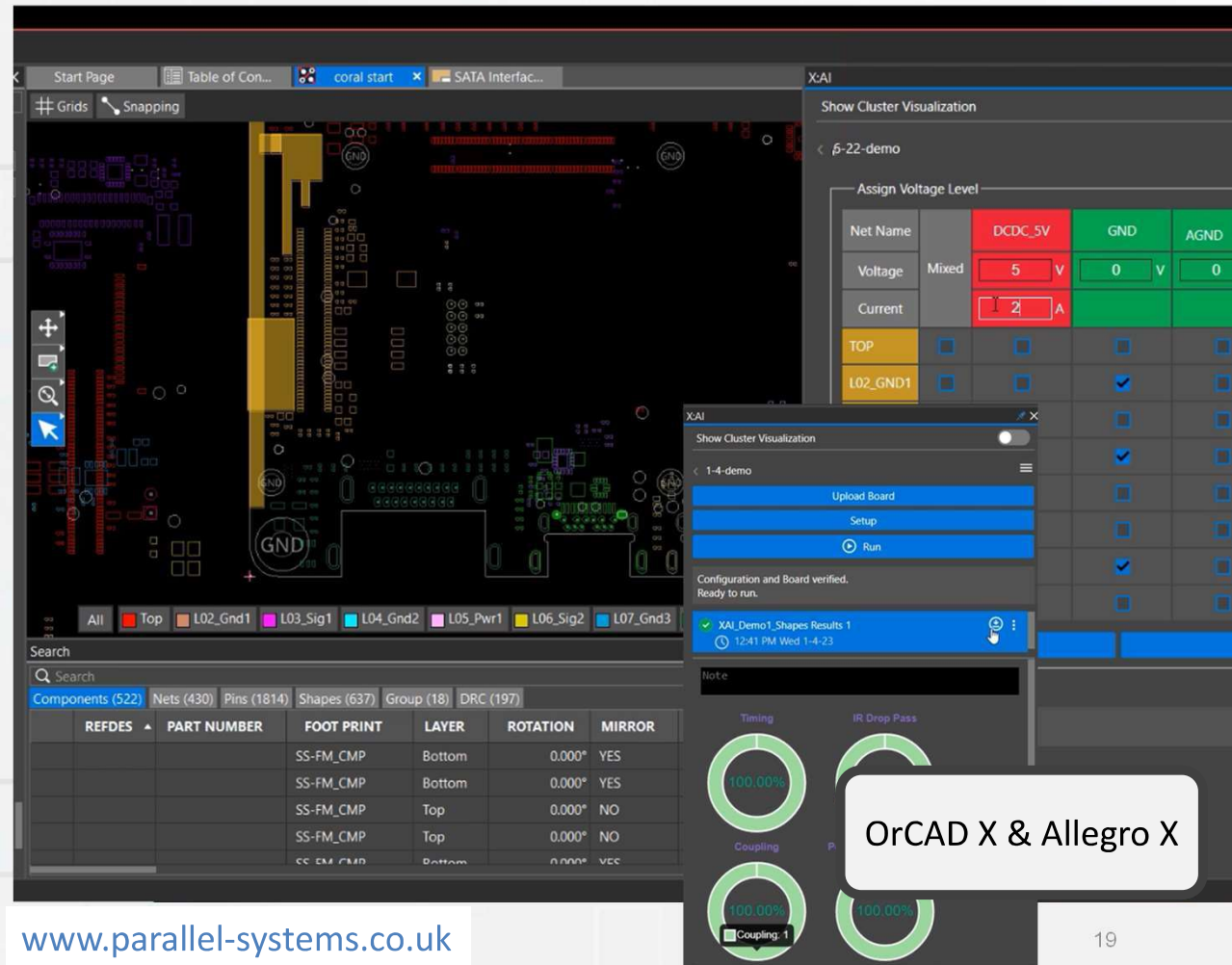
10X+

Productivity



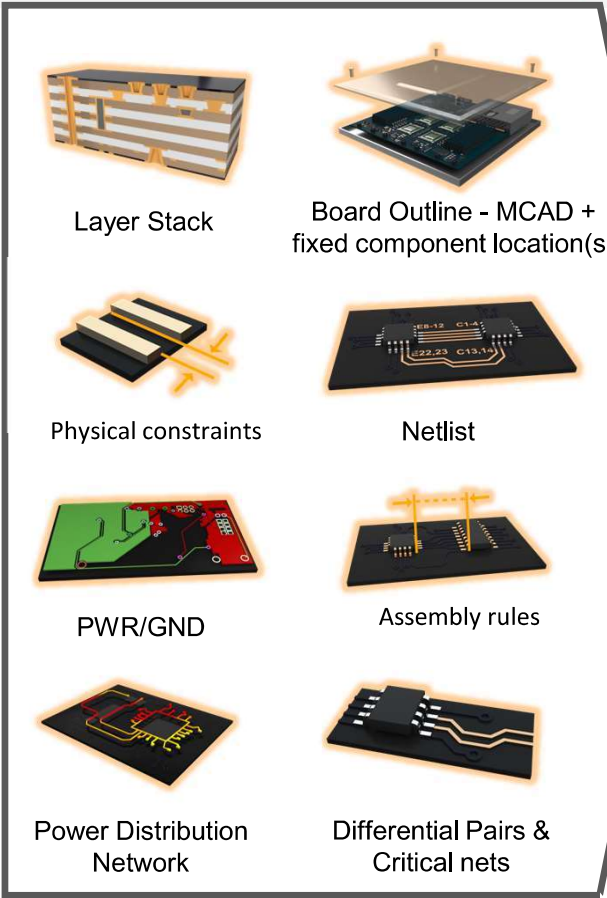
# X AI

- Generative AI Assistant
- Built to perform multiple tasks (placement, routing, plane generation, partial, full)
- Integrated directly inside OrCAD X & Allegro X

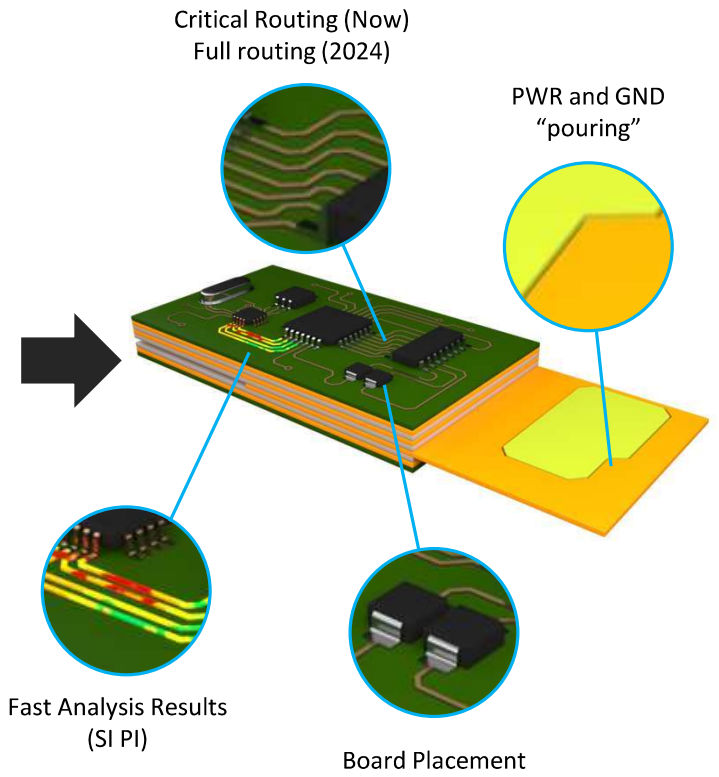
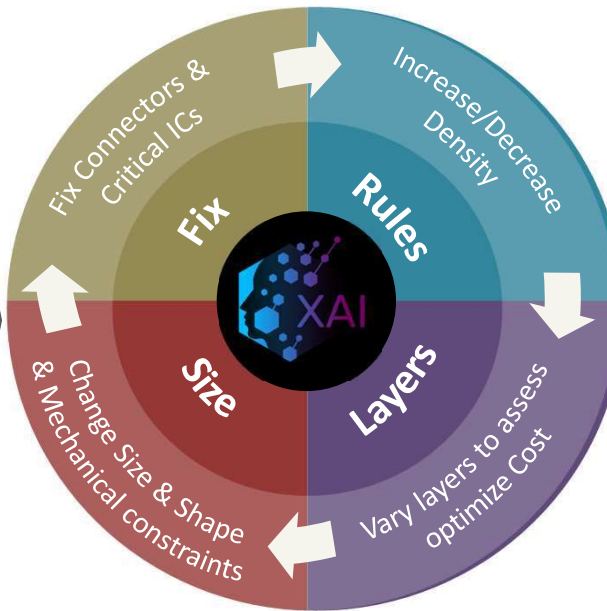


www.parallel-systems.co.uk

# X AI™ Methodology



## Rapid Solution Space Exploration



# X AI Results

PLACEMENT

3 days to  
75 Minutes

WIRELENGTH

12%  
Improved

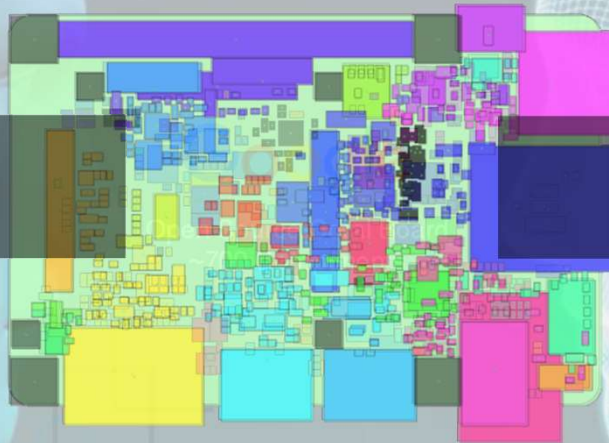
MANUFACTURING

100%  
Compliant

ELECTRICAL  
ANALYSIS

Optimized

Human Alone



w/ X AI

Leverages Cadence OnCloud to  
evaluate 1000s of alternatives

[www.parallel-systems.co.uk](http://www.parallel-systems.co.uk)

# X AI™ Value to PCB Stakeholders

Your AI Assistant



## Engineering Manager

- Increase PCB organization output and efficiency
- Reduce Design TAT



## Electrical Engineer

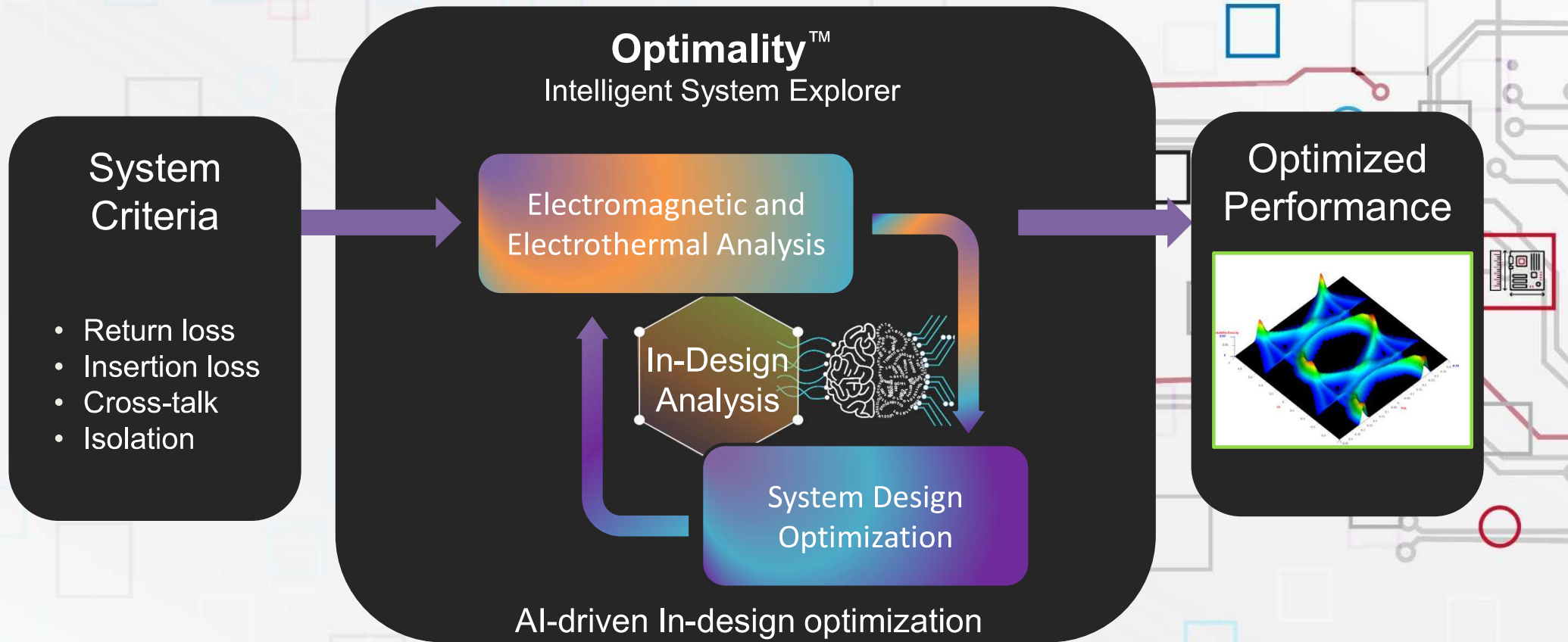
- Expand EE Contribution to PCB Layout
- Experiment with Different Solutions – Explore Design Space



## PCB Designer

- Frees PCB designer to focus on complex PCB problems and multiplies productivity
- X AI provides insights, new ideas, and ability to optimize

# Optimality Intelligent System Explorer

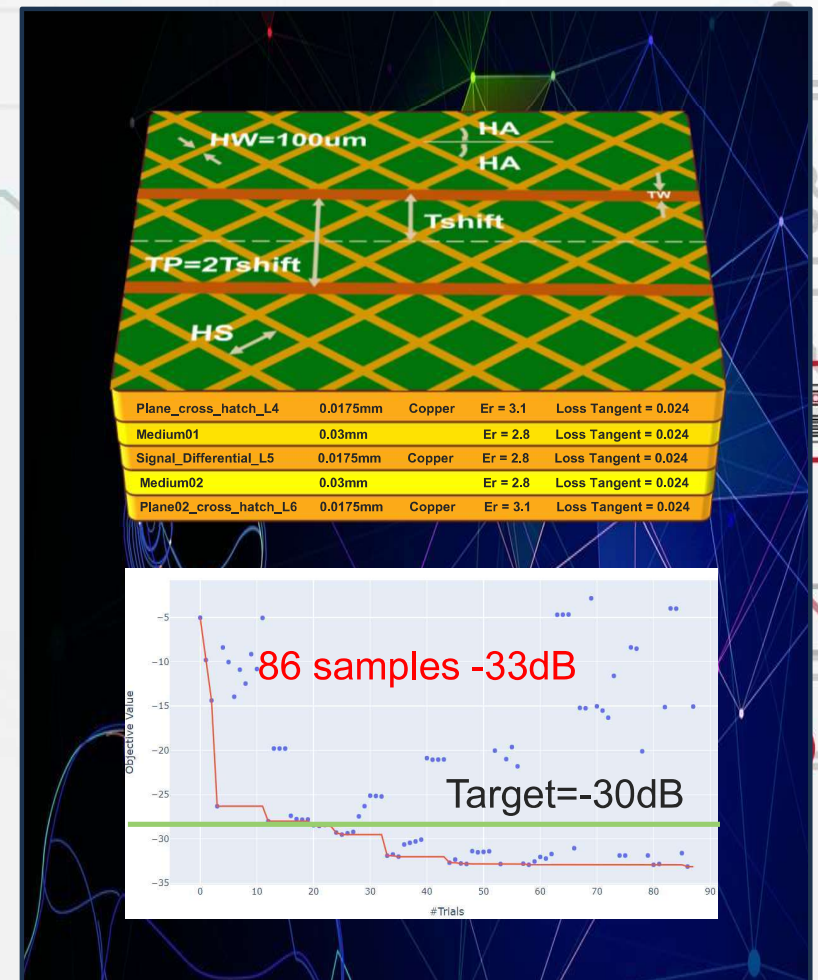


# Optimality™ Intelligent System Explorer

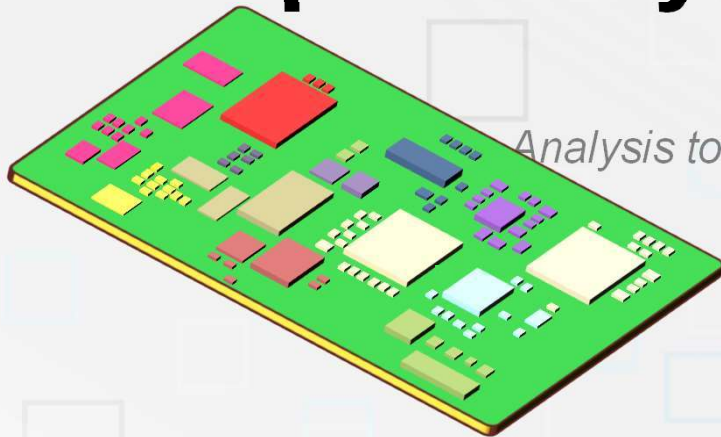
Example:

- Minimize transmission line return loss:
- -30dB target in the frequency band [0GHz-15GHz]
- 5 physical variables: HW, HS, HA, TW, TP
- Brute-force sweeping requires 2,880,000 evaluations (20x20x18x20x20)

[www.parallel-systems.co.uk](http://www.parallel-systems.co.uk)



# Allegro X AI™ and Optimality™ Vision



*Analysis to In-Design Optimization*

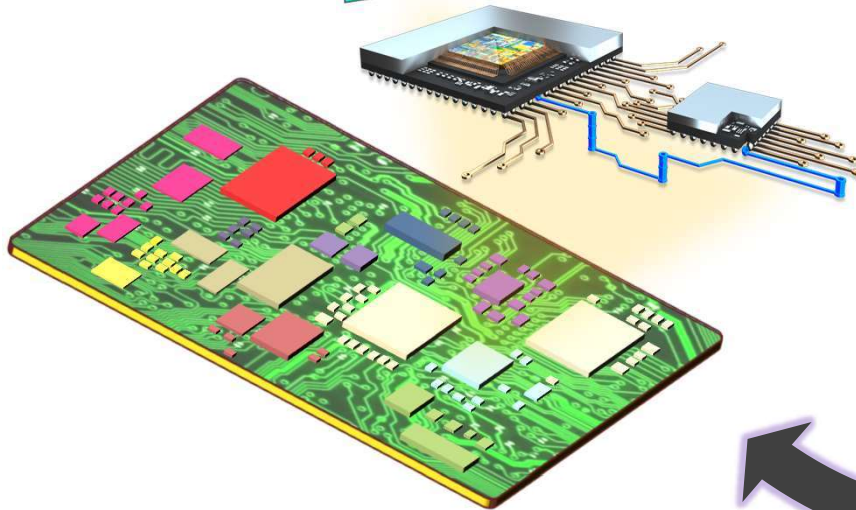
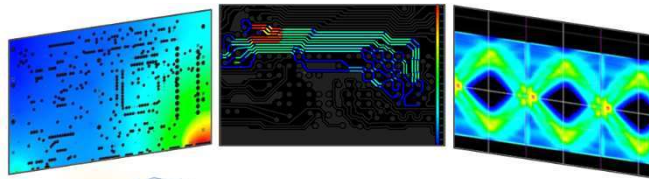
Continuous improvement  
to placement & routing



# Allegro X AI™ and Optimality™ Vision

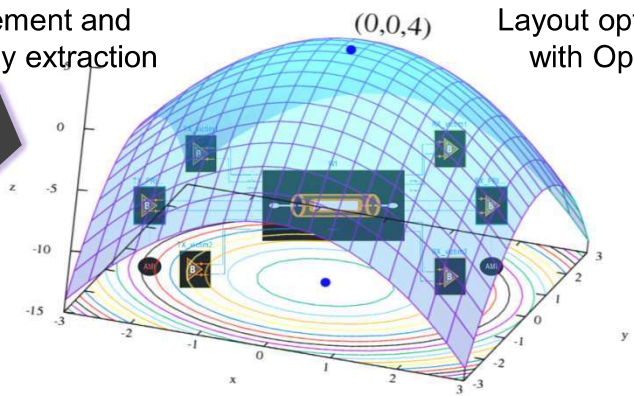
*From In-Design Analysis to In-Design Optimization*

Tighter integration  
with analysis - IDA



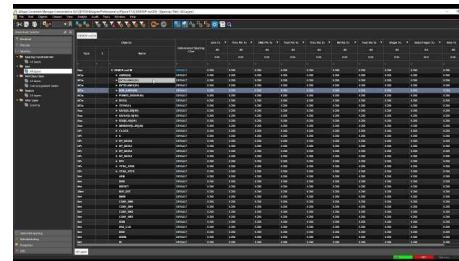
Continuous improvement  
to placement & routing

Placement and  
topology extraction



Layout optimization  
with Optimality

Auto generation of  
constraints

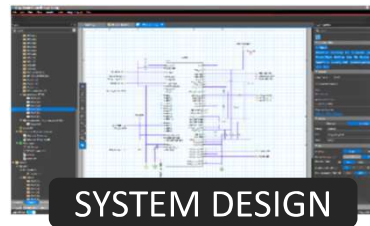
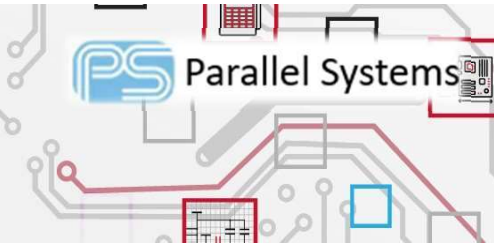


Feed constraints  
back into Allegro X AI



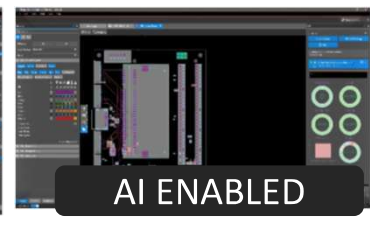
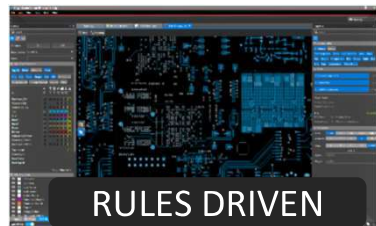
# OrCAD X & Allegro X

## Next Generation PCB Implementation Platform



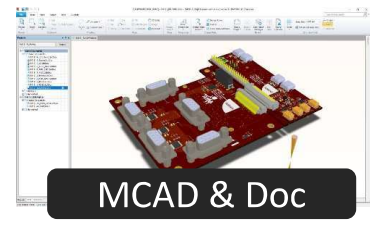
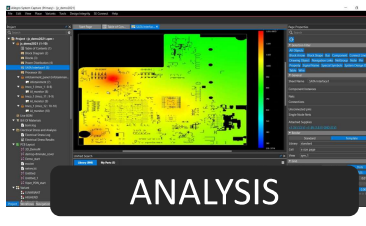
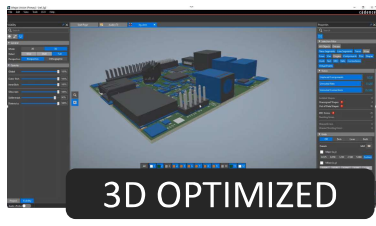
**PERFORMANCE**

- 10x Faster Shapes
- GPU & Parallelization Accelerated



**CAPACITY**

- High-Capacity 3D Engine
- High-Capacity PCB Engine



**CONNECTIVITY**

- Supply Chain Intelligence Built In
- DFM & Simulation Aware Design
- MCAD Integration

**PRODUCTIVITY**

- Next Gen UI/UX for Schematic & Layout
- AI Enabled Generative PCB Design
- Shift-Left Enabled